Wideband, Low-Noise Amplifiers for the Mid-Range SKA

by

Dewald Alewyn Botes

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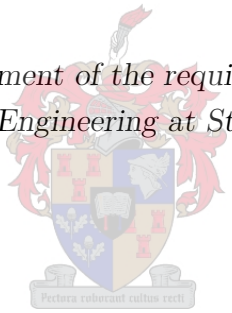

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Declaration

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Abstract

Key words: Wide-band LNA, feedback, Multi-path.

This thesis presents the design, construction and measurement of two wide-band LNA's for the SKA-Mid range (350-1200 MHz). The first wide-band LNA involves the investigation of classic low noise amplifier techniques, which includes basic noise theory, stability analysis, feedback design and the development of sophisticated matching techniques for ultra wide-band performance. Final measurements show a flat gain response equal to 19 dB, with a noise figure of 1.5 dB and an output return loss of 10 dB across the entire bandwidth.

A multi-path cascading concept is introduced for the second low noise amplifier design, which aims to connect two single frequency amplifiers in parallel to operate from 500 to 700 MHz. The design process involves several optimization schemes to realise the matching networks for the cascaded topology and the noise performance of the device was confirmed by using multi-port noise theory. The prototype presents significant bandwidth improvements compared to a single frequency LNA design. Excellent agreement between the simulation and measurement were obtained with a flat gain response of 20 dB across a 2:1 bandwidth, with a low noise figure of 0.95 dB and an output return loss of 13 dB across the operation bandwidth of 400 to 800 MHz.

Opsomming

Sleutelwoorde: Wyeband,Laeruis Versterker, Terugvoer, Multi-Pad

Hierdie tesis behandel die ontwerp, konstruksie en meting van twee wyeband laeruis versterkers vir die SKA - Mid reeks (350–1200 MHz). Die eerste wyeband laeruis versterker, ondersoek klassieke laeruis versterker tegnieke wat insluit basiese ruisteorie, stabiliteit analise, terugvoerontwerp en die ontwikkeling van gevorderde aanpassingstegnieke vir ultra wyeband werkverrigting. Finale metings het 'n plat aanwins van 19 dB, met 'n ruisfiguur van 1.5 dB en 'n uittree-refleksie koëffisiënt van -10 dB oor die hele bandwydte vertoon.

'n Multi-pad konsep word bekend gestel vir die tweede laeruis versterker. Die ontwerp het twee enkel frekwensie laeruis versterkers in parallel verbind om vanaf 500 tot 700 MHz te werk. Die ontwerp proses bevat verskeie optimalisering skemas om die aanpassings netwerke vir die kaskade topologie te realiseer. Die ruissyfer van die versterker is bevestig deur die gebruik van multi-pad ruisteorie. Die prototipe het beduidende bandwydte verbeterings vertoon in vergelyking met 'n enkel frekwensie versterker ontwerp. 'n Uitstekende ooreenkoms tussen die simulasie en meting was verkry met 'n plat aanwins van 20 dB oor 'n 2:1 bandwydte, met 'n laeruisfiguur van 0.95 dB en 'n uittree-refleksie koëffisiënt van -13 dB oor die bandwydte van 400-800 MHz.

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Chapter 1

Introduction

1.1 The SKA Telescope

In the 1930's, Jansky observed the first radio waves originating from the milky way as one of the first forms of possible extraterrestrial communication within the universe [1]. Since then, the radio astronomy science evolved to further study other strange phenomenons in the universe. The radio telescope technology used have taken different forms, for example, the Aricibo telescope [2], High Energy Gamma Ray Astronomy (HEGRA) [3], Röntgen Satellite (ROSAT) [4] and Very Large Array (VLA) [5], which operate at different frequencies in order to view distinct parts of the electromagnetic spectrum. One of the most important figures of merit of a radio telescope is the sensitivity which is defined as follows [6]

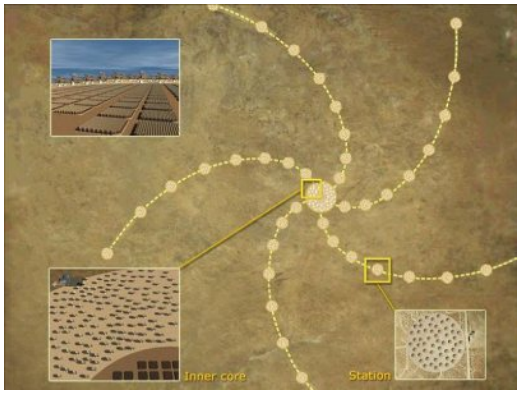
$$Sensitivity = \frac{A_{eff}}{T_{sys}} \tag{1.1}$$

where A_{eff} is the aperture efficiency or total collecting area of the radio telescope and T_{sys} is the system noise temperature measured in Kelvin. The Square Kilometre Array (SKA) aims to be the most sensitive telescope in the world, by maximizing the collecting area to cover a total area of one square kilometre. It furthers aims to improve performance by pushing the boundaries of current technology to operate over a frequency range from 40 MHz to 10 GHz at very low noise temperatures [6].

In order to cover this gigantic frequency range the SKA telescope is divided into three different parts, SKA-Low (40-400 MHz) developed in Australia, SKA-Mid (350-1200 MHz) and several high frequency dishes developed for South Africa. The proposed layout for the dish arrangement in South Africa are shown in Figure 1.1(a) in order to maximise the area [6].

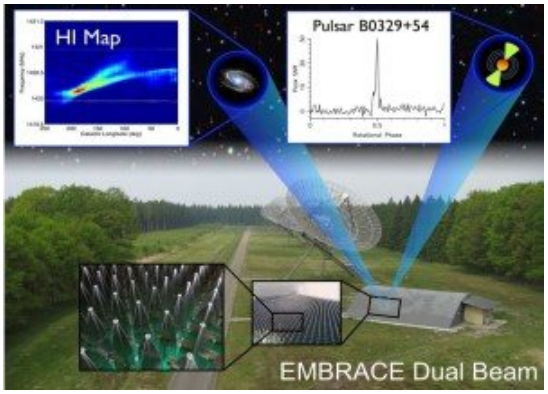
For this thesis the focus is on the Mid Frequency Aperture Arrays (MFAA's) that will be constructed in phase 2 of the project. An artist's impression of these dishes are shown in Figure 1.1(b). Key science goals for the MFAA are to measure the impact of *Dark Energy* on the universe, as well as using the high speed survey capabilities of the MFAA to observe and understand pulsars and other interesting radio transient events as demonstrated in Figure 1.1(c) [7]. In order to achieve these science goals very sensitive receivers are required because in the mid frequency range the system noise temperature T_{sys} is not dominated by the sky noise temperature T_{sky} as is the case for the low frequency aperture array (LAA) [6]. The most important

subsystem from a noise perspective, is the first stage amplifier, designed specifically for optimum noise performance, and consequently referred to as a Low-Noise-Amplifier (LNA).



(a)

(b)



(c)

Figure 1.1: (a) Proposed Layout of SKA [8] (b) Artist's impression of Dense Aperture Arrays [7] (c) Operation of Dense Aperture Arrays [7]

1.2 Wide Band UHF LNAs

1.2.1 Requirements for SKA

For the Square Kilometre Array (SKA) mid-range (350 MHz-1.2 GHz), Low-Noise Amplifiers (LNA's) are required over a very wide band of 3:1. This frequency range poses problems in terms of the technology of implementation, as transmission line circuits are very large, and lumped-element components have low Q-values (or high parasitic resistance). In order to achieve good noise matching over wide bandwidths using the input impedance of a typical wire antenna as source is difficult, as the impedance change significantly over such a bandwidth.

Along with low noise performance and high gain requirements, a crucial parameter in the design is the power consumption of the amplifier, where each of these LNA's will be used in an array configuration consisting of thousands of elements. The design engineer is then faced with a trade off between the three factors of noise, gain and power consumption for ultimate performance. Preliminary specifications of the LNA's for the MFAA are shown in Table 1.1.

Parameter:	Specification:
Frequency(MHz)	350 - 1200
Quantity of required LNA's	55,000,000
T_{sys}	$<$ 38 K
Gain	$>$ 20 dB
Power consumption	<30 mW

Table 1.1: LNA requirements for Mid-Freqeuncy Apperture Array [6]

1.2.2 LNA Performance of Recent LNA's

Recent developments in the LNA technologies are shown in Table 1.2, where it is clear that the requirements for the purposes of the MFAA haven't been accomplished. The designers are constantly faced with the trade off between power consumption which leads to increase in cost and over all noise performance which will improve the sensitivity and the overall capabilities of the SKA radio telescope.

LNA	Bandwidth(GHz)	Gain(dB)	NF(dB)	Power(mW)	Technology
[9]	0.5-2.5	15	0.2	-	mHEMT
[10]	0.7-1.4	15	0.35	-	90nm-CMOS
[11]	0.6-2	16.7-13	0.37-0.79	-	70nm mHEMT
[12]	0.005-2	13.0-22.5	1-1.5	18.81	SiGe HBT
[13]	0.005-4	16-35	1.5-2.8	34.65	SiGe HBT
[14]	0.7-1.8	14.9-18.3	0.56-0.67	40.78	0.25μm SOS
[15]	0.3-1	26-36	0.6-0.75	2880	ATF-34143

Table 1.2: Comparison of different Technology for wide-band UHF LNA

1.3 Objectives

The aim of this work is to design several wide-band low noise amplifiers, for SKA-Mid (350-1200 MHz). The thesis focusses on the following aspects:

- The basic noise theory necessary to understand the effects on the sensitivity of the receiver and a thorough noise analysis of two port networks, including the effect of multi-port noise using the noise correlation matrix.
- Wide-band amplifier design considerations such as device stabilization, incorporation of feedback and the design of sophisticated matching networks.
- Modelling of the amplifiers using state of the art design and simulation software for increased performance.
- Measurement techniques to accurately verify the operation of the wide-band LNA over the band of operation.
- The design, construction and measurement of two wide-band LNA's, achieving 20 dB of gain and an NF of 1.2 dB and 0.95 dB across the band of operation.

1.4 Overview

Chapter 2 consists of the basic noise theory encountered in high frequency electronic systems and the analysis of the noise generated by two port and multi-port devices. In chapter 3 the basic wide-band LNA design considerations are discussed, such as the influence of stability and negative feedback networks on the noise figure of the amplifier. In order to obtain wide-band operation, sophisticated matching schemes are needed and chapter 4 shows several of these techniques with the focus on lumped element networks for arbitrary loads. The design of several wide-band LNA's are demonstrated in chapter 5, where the trade-off between amplifiers with feedback and large matching networks are shown and what would be preferable for the SiGe HBT technology used in the designs. A multi-frequency, multi-path amplifier design is introduced in chapter 6 and the difficulties that arise when such an interesting topology is implemented using standard single frequency amplifiers is discussed. Chapter 7 shows the noise measurement techniques implemented in order to verify the operation of the two wide-band LNA's, as well as measurements of the two prototype LNA's. The work is concluded in chapter 8.

Chapter 2

Fundamental Noise Theory

This chapter discusses the fundamental concepts of noise in electronic systems, focusing on the relevant types of noise that are encountered in a wide band low noise design. First the phenomenon of noise is defined, along with the important difference between the operating bandwidth and noise bandwidth of a component or system.

Secondly different types of noise are presented such as thermal, shot and flicker noise. A detailed guide to the analysis and calculation of noise generated by any two port network are given. Finally, the extension to multi-port networks are shown to be able to quantify the influence of the noise generated by such a structure in a RF communication system.

2.1 Definition of Noise and Noise Bandwidth

2.1.1 Narrowband Noise Signals

The IEEE standard dictionary of Electrical and Electronic Terms [16] defines noise *as unwanted disturbances superposed upon a useful signal that tend to obscure its information content.* Motchenbacher and Connelly [17] interprets noise as any unwanted disturbance or random fluctuation in the signal at any given time. Both these definitions give the indication that noise can not be predicted and influences the information of the desired signal at any given time.

Scientists and engineers have studied the cause of this phenomenon and have found that the source could either be internal or external to the system [18]. Extrinsic noise, for example, can originate from the sun's radiation or the sparking on a fence, any random disturbance in the environment. The internal vibrations of electrons within a material together with fluctuations in the current, inside active components is referred to as intrinsic noise, and also contributes to the overall noise [17, 19].

In order to evaluate these random signals, we consider the noise signals to be a stochastic[1], band-limited around the operating frequency f_0, with a random amplitude and phase. Mathematically,

[1] **Stochastic process:** A set of random variables that take on random values in time [20].

narrow-band noise signals can be written as [20]

$$y(t) = X(t)e^{j(2\pi f_0 t + \theta(t))} \tag{2.1}$$

where X(t) is the amplitude and $\theta(t)$ is the random phase of the signal at a given time. The average value of the signal is zero due to its stochastic nature. Therefore the only way to quantify the amount of noise added to the system, is to consider the mean squared value of the signal, often denoted as $\overline{i^2}$. The mean squared value of a signal can be written as [18]

$$< ii^* >= \lim_{T\to\infty} \frac{1}{T} \int_0^T i(t)i^*(t)dt \tag{2.2}$$

where T is equal to one period of the signal. For the remainder of this chapter and for the noise analysis to follow the mean squared value of the signal is the preferred quantity in order to aid with the classification of the amount of noise added to the system.

2.1.2 Noise Bandwidth

The definition of the noise bandwidth (Δf) for a general microwave structure is very different from the half power bandwidth (B) typically used in amplifiers or filters. According to [17] the noise bandwidth can be defined as

$$\Delta f = \frac{1}{G_0} \int_0^\infty G(f)df \tag{2.3}$$

where $G(f)$ is the available power gain as a function of frequency and G_0 is the peak available power gain. Equation (2.3) states that Δf is equal to the ideal rectangular power transfer characteristic such that the output noise power is equal to total noise power of the real circuit[18].

A graphical representation for the calculation of the noise bandwidth is shown in Figure 2.1(a). The blue line indicates a theoretical available gain response of an amplifier and the noise bandwidth is then equal to the area indicated by the red dotted line in Figure 2.1(a). This is the point where the area of the total noise power transmitted by the actual response equals the ideal square characteristics indicted by Δf.

The noise bandwidth starts to approximate the half-power bandwidth, if the transfer power S_{21} of the amplifier have a rectangular characteristic. This square response occurs when an amplifier consists of multiple stages or when a single stage amplifier has more than four poles in its matching networks to yield a approximately rectangular response. The following equation estimates the error made when assuming that $\Delta f \approx B$ and can be written as [18]

$$\Delta f = \frac{B}{\sqrt{2^{\frac{1}{2}} - 1}} \int_0^\infty \left(\frac{1}{x^{2n}}\right)^m dx \tag{2.4}$$

where m is the total number of stages in the amplifier design and n is the number of poles in the matching network. Figure 2.1(b) shows the response of a single stage amplifier with a five pole matching network.

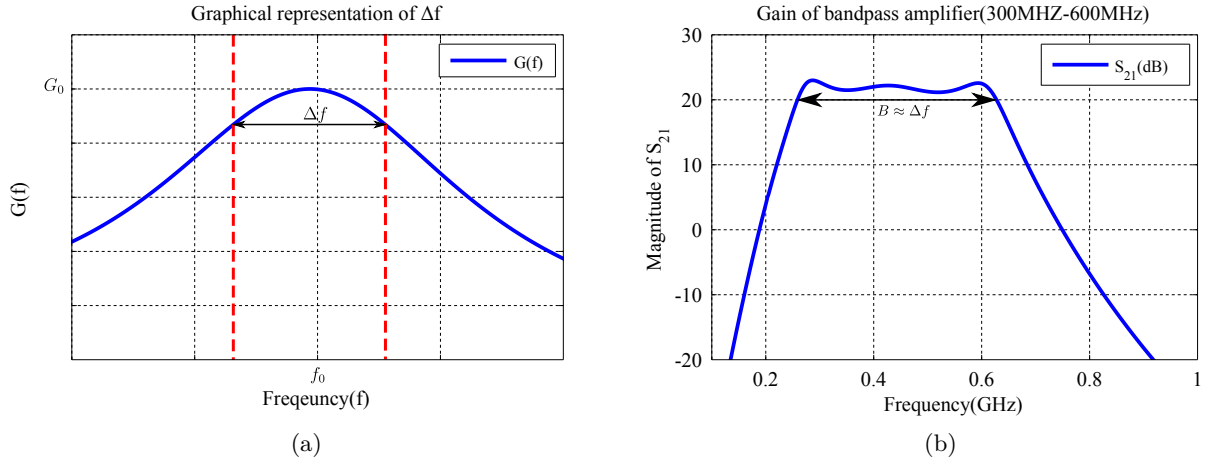


Figure 2.1: Noise bandwidth representation (a) Graphical (b) Approximation

The blue line in Figure 2.1(b) shows the gain of the amplifier.For this gain function, the error made according to equation (2.4) $\frac{\Delta f}{B} = 1.05$. This shows that for a single stage amplifier with 5 pole matching network, it is possible to assume that the noise bandwidth is equal to the half-power bandwidth.

2.2 Different Types of Noise

2.2.1 Thermal Noise

Johnson observed the first random vibration of charged carriers that caused a variation in the output voltage of a resistor with open terminals in 1928 (see Figure 2.2(a)). This discovery lead Nyquist to a mathematical description of thermal noise in the same year. For this reason thermal noise is also called Johnson or Nyquist noise [18]. Consider a noisy resistor at temperature T(K) as shown in Figure 2.2(b)

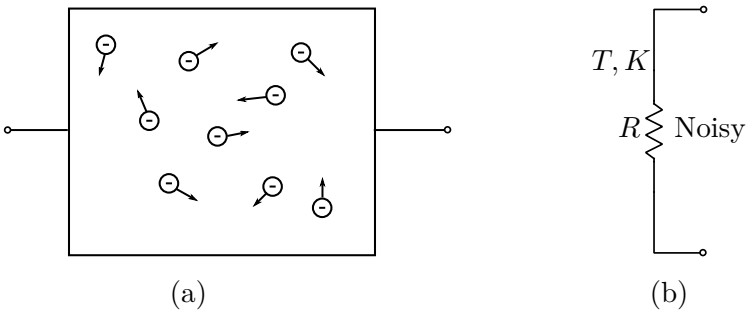


Figure 2.2: (a) Electrons inside a conductor moving in random motion (b) Noisy Resistor at temperature T

If the resistor‘s temperature is above absolute zero kelvin, then the charge carriers starts to move around and cause an instantaneous noise voltage across the terminals of the resistor. The noisy resistor are modelled with its Thevenin equivalent circuit under open circuit conditions as

a noiseless resistor with a noise voltage source $\overline{v_n}$ as shown in Figure 2.3(a). A mathematical description of this random noise voltage can be written as [21]

$$\overline{v_n} = \sqrt{\frac{4hf_0\Delta fR}{e^{\frac{hf_0}{kT}} - 1}} \tag{2.5}$$

where h = Planck's constant (6.0626×10^{-34}J-sec), k = Boltzmann's constant (1.380×10^{-23}J/K), T = Temperature in kelvin (K), f_0 is the centre frequency in Hz, R is the resistance in Ω and – indicates an average value. For microwave frequencies the ratio $\frac{hf_0}{kT} << 1$ and the term $e^{\frac{hf_0}{kT}} - 1$ can be approximated by a Rayleigh-Jeans approximation [22, 17] which reduces equation (2.5) to

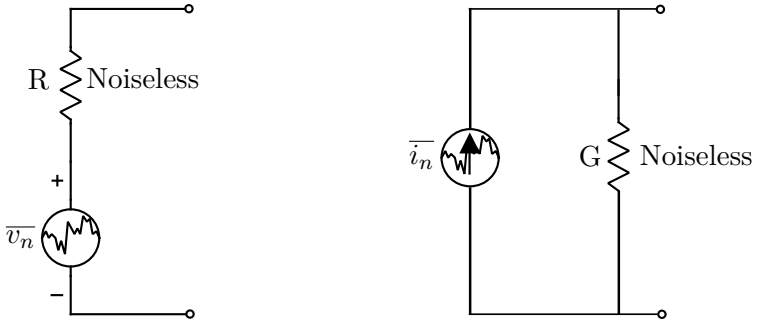
$$\overline{v_n} = \sqrt{4kT\Delta fR} \tag{2.6}$$

Depending on the application, the noisy resistor could also be modelled as a Norton equivalent circuit under short circuit conditions as shown in Figure 2.3(b). The random noise current $\overline{i_n}$ can be written as [17]

$$\overline{i_n} = \sqrt{4kT\Delta fG} \tag{2.7}$$

where G is the conductance of the noisy resistor ($G = \frac{1}{R}$). If a noiseless load is connected to the output terminals of the resistor in Figure 2.3(a) or (b) then the available noise power measured at the output terminals can be written as [19]

$$N_t = \frac{\overline{v_n^2}}{4R} = \frac{\overline{i_n^2}}{4G} = kT\Delta f \tag{2.8}$$



(a) (b)

Figure 2.3: (a) Thevenin equivalent circuit of noisy resistor (b) Norton equivalent circuit of noisy resistor

From equation (2.5) and (2.8) it is important to note that both results are proportional to the noise bandwidth Δf. This means that if your device works over a wider bandwidth more thermal noise is added to the system up to the Raleigh-Jeans limit [18], and less noise is added when the bandwidth δ is decreased.

Another observation is that the operating temperature T of the device determines the amount of noise added to the system. Therefore, LNA's are often cooled down with cryogenic coolers in order to reduce the noise added to the device.

2.2.2 Shot Noise

In active devices, such as diodes and transistors, the fluctuations of the current on the output terminals of the device generates noise called shot noise. This non-linear behaviour is caused by the charge carriers as they cross the potential barrier of the semiconductor device [18]. According to [17] the rms shot noise current across a general diode junction can be defined as

$$\overline{i_{sh}} = \sqrt{2qI_{DC}\Delta f} \tag{2.9}$$

where q is the charge of an electron(1.602×10^{-19} Coulombs) and I_{DC} is the direct current across the junction of a typical semiconductor device.

For amplifier circuits the shot noise originates in the pn-junction of the bipolar junction transistor (BJT). A noise model of this device in its forward biased state is shown in Figure 2.4

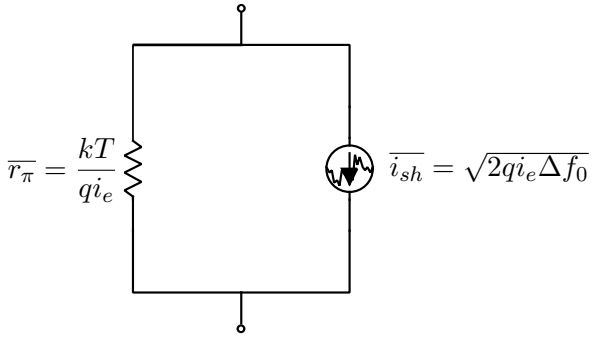


Figure 2.4: A Shot Noise model of a forward biased BJT

In Figure 2.4 the emitter current can be evaluated by two components, namely, the forward biased emitter current and the reversed biased current [17]

$$\begin{aligned} i_e &= i_{e1} + i_{e2} \\ &= -i_s + i_s e^{\frac{qV_{BE}}{kT}} \end{aligned} \tag{2.10}$$

If the device is reverse biased, i_{e2} is zero and the noise current is equal to $\overline{i_{e1}}$. If the transistor is forward biased i_{e2} dominates and the total shot noise current is always the mean value, given by [17]

$$\overline{i_{sh}^2} = 4qi_s\Delta f \tag{2.11}$$

2.2.3 Flicker Noise

Flicker Noise, also known as low frequency or $1/f$ noise, have the power density spectrum of pink noise which can be written as [18]

$$S_f = \frac{1}{f^\alpha} \tag{2.12}$$

where α has been observed to take on values from 0.8 to 1.3 for a variety of devices. The cause of flicker noise is from various material imperfections, for example studies in metal-oxide-semiconductor-field-effective-transistor (MOSFET) have shown that the cause could originate in the lattice structure of the device which is caused by the random mobility of the electrons inside the structure [23].

The influence of flicker noise is determined by comparing the magnitude of the flicker noise with the magnitude of the thermal noise for the selected frequency range. As an example, a theoretical power density spectrum is calculated for the flicker noise as shown by the blue line in Figure 2.5. Assuming that the thermal noise floor indicated by the red line is at -100 dB for the frequency range, the corner frequency f_c which is the intersection point between the thermal and flicker noise is determined as indicated in Figure 2.5.

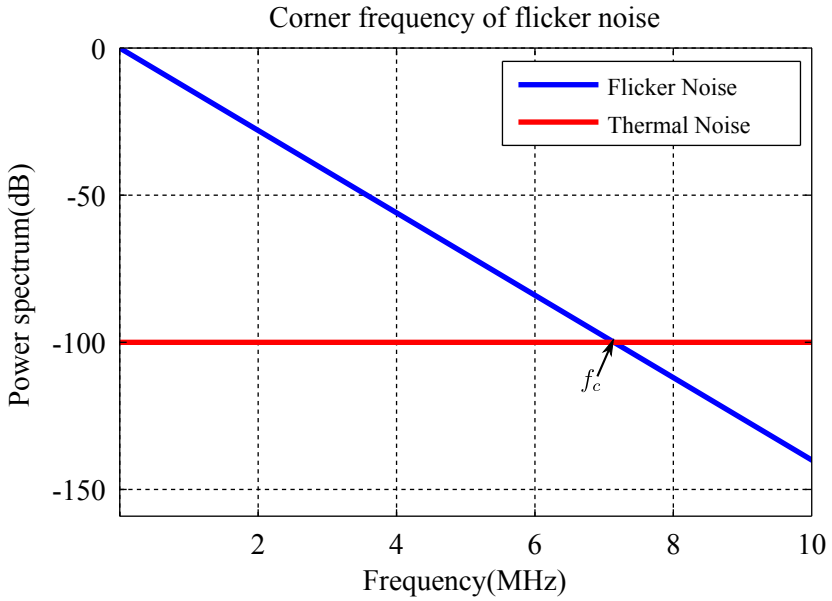


Figure 2.5: Corner frequency of flicker noise

If the thermal noise is much larger than the flicker, the effect can be neglected which is the case for high frequency amplifiers, where the thermal noise is much higher than the flicker noise. It is still important to know about the occurrence of flicker noise in system level design because mixers can up convert the flicker noise to the higher frequencies, influencing the noise figure of the system [18].

2.3 One Port Noise Characterization

It is desired to classify the total noise from a device or system as a single quantity, since there are other sources of noise than just thermal and shot noise contributing to the total noise in the system. From equation (2.6) there are two options to do this, either the temperature T is kept constant and the change in output voltage $\overline{v_n}$ is classified according to an equivalent

resistance, or the resistance can be kept constant and the fluctuating voltage $\overline{v_n}$ is represented by an equivalent temperature [19].

2.3.1 Equivalent Noise Resistance

As shown in Figure 2.3, the noise generated by the circuit can be modelled as a noise source $\overline{v_n}$ in series with the noiseless resistor R which represent the impedance of the circuit. The difference compared with the thermal noise is that all the different noise sources is represented by a fictitious resistor R_n which is different to the physical value R, since other noise sources also adds to the overall noise voltage $\overline{v_n}$ measured at the terminal of the circuit.

A characteristic of R_n is that it can be used to distinguish between the thermal noise generated and the other noise sources in the circuit. Unfortunately this quantity can not tell the other noise sources apart but it can be used to visualise the effect of the additional noise sources. Mathematically, the noise resistance can be written as [19]

$$R_n = \frac{\overline{v_n^2}}{4kT_0\Delta f} \tag{2.13}$$

where $T_0 = 290K$ and $\Delta f = 1Hz$ which means that R_n is a spot noise value with a bandwidth of 1 Hz. The reason the Δf is chosen to be equal to 1 Hz, is because R_n changes with frequency and if Δf is chosen very small it becomes independent of frequency and the variation in the noise voltage v_n is also smaller.

2.3.2 Equivalent Noise Temperature

As shown by equation (2.8) the available noise power generated by a one port does not depend on its physical value. Thus another representation of the noise generated by the one port is the equivalent noise temperature T_e and can be written as [19]

$$T_e = \frac{\overline{v_n^2}}{4kR\Delta f} \tag{2.14}$$

where R represents the physical value of the resistor in Ω. The value obtained by the equivalent noise temperature is a fictitious value which represents the noise of the oneport and it can not be compared to the environmental temperature, except when the noise is thermal in nature.

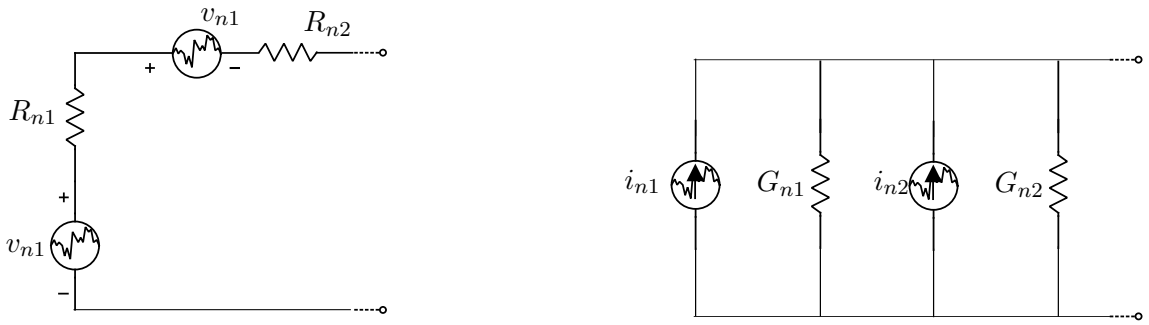
2.3.3 One Port Calculations

Consider a system with multiple elements in series, where the noise from each element can be represented by an equivalent noise resistance R_n, as shown in Figure 2.6(a). The total noise from the system can be combined by using superposition as follows [19]

$$R_n = \sum_{j=1}^{N} R_{n,j} \tag{2.15}$$

$$\overline{v_n^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2} + \cdots + \overline{v_{nN}^2} \tag{2.16}$$

where N is the total number of elements in series. It is important to note that, for this case, all the noise sources $v_{n1}..v_{nN}$ from the individual elements are assumed to be uncorrelated. If this is not the case, and the noise sources are correlated and a correlation needs to be defined as explained in section 2.5.



(a) (b)

Figure 2.6: One port noise calculations using super position

The system may also be presented by equivalent noise conductances in parallel as shown in Figure 2.6 (b). Once again super position can be used under the assumption that the individual noise sources are uncorrelated, and can be written as [19]

$$G_n = \sum_{j=1}^{N} G_{n,j} \tag{2.17}$$

$$i_n^2 = i_{n1}^2 + i_{n2}^2 + \cdots + i_{nN}^2 \tag{2.18}$$

where G_n is the equivalent noise conductance of the entire one port circuit and the subscripts j indicates the individual elements.

2.4 The Noise Figure

2.4.1 Noise Figure Definition

According to [22] the noise factor of an amplifier or subsystem is defined as the degradation in the signal to noise ratio between the input and output port, given by

$$F = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{1}{G_T} \cdot \frac{N_{out}}{N_{in}} \tag{2.19}$$

where S = Signal power, N = Noise power and G_T = Transducer gain. It is important to note that S_{in} and N_{in} represent available power. As an example, consider the circuit shown in Figure 2.7, where a signal is applied at the input port of a noisy amplifier with a gain of G_T. The noise factor of the component is calculated from equation (2.19) and the noise power measured at the output port of the amplifier consists of two uncorrelated components

$$N_{out} = N_{out}(source) + N_{out}(DUT) \tag{2.20}$$

where $N_{out}(source)$ is the output noise power generated by the source and amplified by an ideal amplifier(all other noise sources ignored). $N_{out}(DUT)$ is the output noise power of the internal

noise sources of the amplifier and the output noise power can be substituted into equation (2.19), resulting in [22]

$$F = 1 + \frac{N_{out}(DUT)}{N_{out}(source)} \tag{2.21}$$

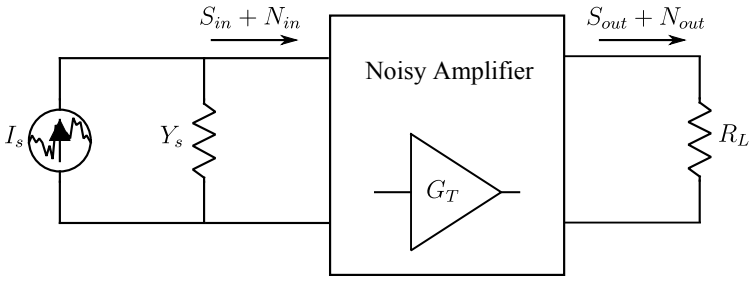


Figure 2.7: Noisy amplifier excited by current source

The noise figure(NF) is equal to the noise factor expressed in decibels and can be written as

$$NF = 10\ Log(F) \tag{2.22}$$

2.4.2 The Noise Figure in Terms of Noise Parameters

In amplifier design it is useful to characterize the noise figure of the device according to its noise parameters, equivalent noise resistance R_n, minimum noise figure NF_{min} and optimum noise admittance Y_{opt}. These quantities are usually supplied by vendors and assists in the analysis and design of a low noise amplifier. This section shows how to derive the noise figure in terms of these parameters based on work from [24].

Consider the circuit shown in Figure 2.8, where a noise current source i_s with admittance Y_s excites an amplifier. A noisy two port can be presented by its noiseless counterpart, with the noise sources v_n,i_n of the device transferred to the input of the amplifier (see section 2.5.2).

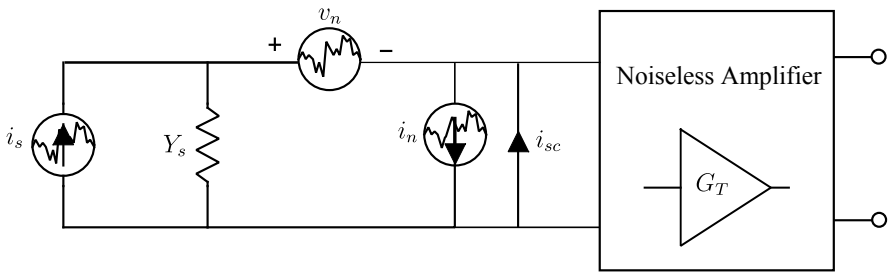


Figure 2.8: Noiseless amplifier excited by a current source with internal noise sources referred to the input

The output noise power can be determined by measuring the short circuit current at the input port. The noise factor can then be calculated from equation (2.19) as follows

$$F = \frac{\overline{i_{sc}^2}}{\overline{i_s^2}} \tag{2.23}$$

where i_{sc} is the short circuit current at the input of the amplifier. It is important to note that the currents and voltages for this derivation represent mean values unless otherwise stated. By writing a node equation at the input of the amplifier the mean squared short circuit current can be expressed as

$$\begin{aligned} i_{sc} &= v_n Y_s + i_n - i_s \\ \Rightarrow \overline{i_{sc}^2} &= \overline{i_s^2} - \overline{2i_s(i_n + v_n Y_s)} + \overline{(i_n + v_n Y_s)^2} \end{aligned} \tag{2.24}$$

Assuming that the noise generated by the source and the amplifier are uncorrelated

$$\overline{2i_s(i_n + v_n Y_s)} = 0 \tag{2.25}$$

which simplifies equation (2.24) to

$$\overline{i_{sc}^2} = \overline{i_s^2} + \overline{(i_n + v_n Y_s)^2} \tag{2.26}$$

For the noise generated by the amplifier there normally exists some correlation between the sources v_n, i_n, therefore i_n can be divided in two parts

$$i_n = i_{nu} + i_{nc} \tag{2.27}$$

where the subscripts nu and nc are for the correlated and uncorrelated noise generated by the source i_n, respectively. We can define the correlation between the sources v_n and i_{nc} in terms of a correlation admittance Y_c

$$Y_c = \frac{i_{nc}}{v_n} \tag{2.28}$$

Y_c is not a physical admittance in the circuit and is purely for the calculation of the noise figure. By substituting equation (2.28) into equation (2.27) and multiplying with v_n^* the correlation admittance can be written in terms of the amplifier noise sources as follows

$$\begin{aligned} i_n &= i_{nu} + v_n Y_c \\ \Rightarrow \overline{v_n^* i_n} &= \overline{i_{nu} v_n^*} + Y_c \overline{v_n^2} \\ Y_c &= \frac{\overline{v_n^* i_n}}{\overline{v_n^2}} \end{aligned} \tag{2.29}$$

Substituting equation (2.27) into (2.23) the noise factor is written as

$$F = 1 + \frac{\overline{(i_{nu} + (Y_c + Y_s)v_n)^2}}{\overline{i_s^2}} \tag{2.30}$$

We assume that the noise generated by the source is thermal in nature (see section 2.2.1) and the source noise current can be written as

$$\overline{i_s^2} = 4kTG_s\Delta f \tag{2.31}$$

The mean squared noise voltage and uncorrelated noise current can be written in terms of the equivalent noise resistance(R_n) and conductance(G_u)

$$\overline{v_n^2} = 4kTR_n\Delta f \tag{2.32}$$

$$\overline{i_{nu}^2} = 4kTG_u\Delta f \tag{2.33}$$

These quantities can be substituted into equation (2.30) and simplified to give

$$F = 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s}[(G_s + G_c)^2 + (B_s + B_c)^2] \tag{2.34}$$

where $Y_c = G_c + jB_c$ and $Y_s = G_s + jB_s$. The final step in the derivation is to determine F_{min}. From equation (2.34) it is clear that a minimum noise factor can be achieved by setting

$$B_s = -B_c \tag{2.35}$$

and the dependence of F on G_s can be minimized as follows

$$\left.\frac{dF}{dG_s}\right|_{B_s=-B_c} = 0 \tag{2.36}$$

$$-\frac{G_u}{G_s^2} + R_n\left(\frac{2G_s(G_s+G_c) - (G_s+G_c)^2}{G_s^2}\right) = 0 \tag{2.37}$$

$$\Rightarrow G_s = \sqrt{G_c^2 + \frac{G_u}{R_n}} \tag{2.38}$$

The optimum noise admittance can then be defined as

$$\begin{aligned} Y_{opt} &= G_{opt} + jB_{opt} \\ &= \sqrt{G_c^2 + \frac{G_u}{R_n}} - jB_c \end{aligned} \tag{2.39}$$

where the minimum noise figure is reached when the source admittance is equal to the optimum noise admittance in equation (2.39)

$$\begin{aligned} F_{min} &= F|_{Y_s=Y_{opt}} \\ \Rightarrow F_{min} &= 1 + 2R_n(G_{opt} + G_c) \end{aligned} \tag{2.40}$$

The minimum noise figure can then be substituted to give the noise factor in terms of the noise parameters as follows

$$F = F_{min} + \frac{R_n}{G_s}[(G_s - G_{opt})^2 + (B_s - B_{opt})^2] \tag{2.41}$$

Equation (2.41) can be used to quickly calculate the noise factor of a two port network given a set of noise parameters and source admittance.

2.5 Noise Correlation matrix

2.5.1 Definition of The Noise Correlation Matrix

The noise correlation matrix represents the correlation between the noise sources of a noisy two port. As described by Rothe and Dahlke [25], a noisy two port can be broken up into a noiseless two port with noise generators x_1, x_2 at the input and output depending on the type of configuration. It is very important to note than when dealing with the correlation matrix the signals are assumed to be narrowband signals operating at a frequency f with a random

amplitude and phase. In the time domain the autocorrelation of one of these noise signals can be defined as [20]

$$R(t) = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x(t+\tau)x^*(\tau)d\tau \tag{2.42}$$

At time $t = 0$, $R(0)$ is often denoted as [20]

$$R(0) = \overline{x(t)x^*(t)} = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x(\tau)x^*(\tau)d\tau \tag{2.43}$$

and the cross-correlation of the two noise signals, at time t=0 can be written as [20]

$$\overline{x_1x_2^*} = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x_1(\tau)x_2^*(\tau)d\tau \tag{2.44}$$

The total power of the two noise signals is equal to the sum of the auto and cross-correlation of the two signals at time t=0 and can be written as [20]

$$\begin{aligned} N_t = R(t=0) &= \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} [x_1 + x_2] \cdot [x_1^* + x_2^*]d\tau \\ &= \overline{x_1x_1^*} + \overline{x_1x_2^*} + \overline{x_2x_1^*} + \overline{x_2x_2^*} \end{aligned} \tag{2.45}$$

If the mean power of the two noise signals are combined in matrix form, the correlation matrix is formed and can be written as [18]

$$[C] = \begin{bmatrix} \overline{x_1x_1^*} & \overline{x_1x_2^*} \\ \overline{x_2x_1^*} & \overline{x_2x_2^*} \end{bmatrix} \tag{2.46}$$

where the diagonal terms are equal to the auto-correlation of the signals and the off-diagonal entries are the cross-correlation of the noise signals. In general, to analyse a signal in the frequency domain, the well known Fourier transform is used [20]

$$X(\omega) = \mathfrak{F}[x(t)] = \int_{-\infty}^{\infty} x(t)e^{-j\omega t}dt \tag{2.47}$$

Taking the Fourier transform of the auto correlation function for one of the noise sources and assuming that $x_1(t)$ and $x_2(t)$ are infinite energy signals, the following relationship can be established [20]

$$\mathfrak{F}[R(t)] = \int_{-\infty}^{\infty} \left[\lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x(t+\tau)x^*(\tau)d\tau \right] e^{-j\omega t}dt \tag{2.48}$$

$$= \lim_{T\to\infty} \frac{1}{T} X(\omega)X^*(\omega) \tag{2.49}$$

This result is very important and is known as the power spectral density (PSD) denoted as $S_{xx}(\omega)$. The next step links the time domain to the frequency domain. If the inverse Fourier transform is taken from S_{xx} and evaluated at time t=0, the following result is obtained

$$N_t = R(0) =< xx^* >= \int_{-\infty}^{\infty} S_{xx}(f)df \tag{2.50}$$

Equation (2.50) states that the noise power in the signals can either be obtained by evaluating the auto and cross correlation at time t= 0, or by integrating S_{xx} over the noise bandwidth which is usually 1 Hz.

2.5.2 Noise Correlation Matrix Representations and Transformations

In electronic engineering the analysis of a general two port is done by means of any of the common network representations, such as Z-parameters, Y-parameters and ABCD-parameters. Rothe and Dahlke [25] derived an equivalent noise representation for each of the well-known two port networks, shown in Figure 2.9. Each of these noise sources are correlated, and the correlation matrix for each representation can be written as follows

$$[C_Y] = \begin{bmatrix} \overline{i_{n1}i_{n1}^*} & \overline{i_{n1}i_{n2}^*} \\ \overline{i_{n2}i_{n1}^*} & \overline{i_{n2}i_{n2}^*} \end{bmatrix} \tag{2.51}$$

$$[C_Z] = \begin{bmatrix} \overline{v_{n1}v_{n1}^*} & \overline{v_{n1}v_{n2}^*} \\ \overline{v_{n2}v_{n1}^*} & \overline{v_{n2}v_{n2}^*} \end{bmatrix} \tag{2.52}$$

$$[C_T] = \begin{bmatrix} \overline{v_n v_n^*} & \overline{v_n i_n^*} \\ \overline{i_n v_n^*} & \overline{i_n i_n^*} \end{bmatrix} \tag{2.53}$$

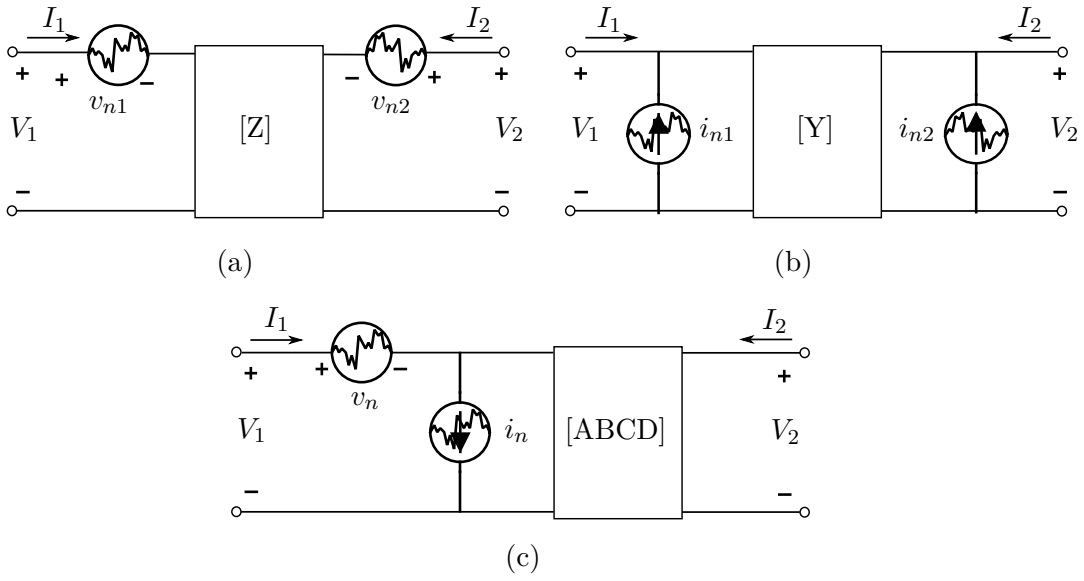


Figure 2.9: (a) Z-matrix noise representation (b) Y-matrix noise representation (c) ABCD-matrix noise representation

Hillbrand and Russer [26] showed that simple transformation between the different representations using the transformation matrices in Table 2.1 are possible. As an example $[C_T]$ is transformed to $[C_Y]$, where the chain correlation matrix is obtained from vendor supplied data as explained in section 2.5.3. The first step is to write the relationship between the voltage and currents for each representation shown in Figure 2.9(b) and (c) as follows

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} + \begin{bmatrix} v_n \\ i_n \end{bmatrix} \tag{2.54}$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} i_{n1} \\ i_{n2} \end{bmatrix} \tag{2.55}$$

Setting the voltages V_1 and V_2 equal to zero in equation (2.54) and (2.55), results in the following relationship

$$\begin{bmatrix} i_{n1} \\ i_{n2} \end{bmatrix} = \begin{bmatrix} \frac{-D}{B} & 1 \\ \frac{1}{B} & 0 \end{bmatrix} \cdot \begin{bmatrix} v_n \\ i_n \end{bmatrix} \tag{2.56}$$

$$\begin{bmatrix} v_n \\ i_n \end{bmatrix} = \begin{bmatrix} 0 & B \\ 1 & D \end{bmatrix} \cdot \begin{bmatrix} i_{n1} \\ i_{n2} \end{bmatrix} \tag{2.57}$$

Now that the transformation matrix has been established, the following relationship can be used to transform from $[C_T]$ to $[C_y]$

$$[C_Y] = \begin{bmatrix} \frac{-D}{B} & 1 \\ \frac{1}{B} & 0 \end{bmatrix} \cdot [C_T] \cdot \begin{bmatrix} \left(\frac{-D}{B}\right)^* & \left(\frac{1}{B}\right)^* \\ 1 & 0 \end{bmatrix} \tag{2.58}$$

$$\Rightarrow [C_Y] = R \cdot [C_T] \cdot R^\dagger \tag{2.59}$$

where the † is the Hermitian or conjugate transpose.

Resulting Representation	**Original Representation**		
	Admittance	Impedance	Chain
Admittance	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$	$\begin{bmatrix} -y_{11} & 1 \\ -y_{21} & 0 \end{bmatrix}$
Impedance	$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -z_{11} \\ 0 & -z_{21} \end{bmatrix}$
Chain	$\begin{bmatrix} 0 & B \\ 1 & D \end{bmatrix}$	$\begin{bmatrix} 1 & -A \\ 0 & -B \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

Table 2.1: Transformation matrices between Admittance, Impedance and Chain representations

Another useful attribute of the correlation matrix is that individual 2-port networks can easily be combined depending on the configuration type [26].

$$[C_Y] = [C_{Y1}] + [C_{Y2}] \quad (Parrallel) \tag{2.60}$$

$$[C_Z] = [C_{Z1}] + [C_{Z2}] \quad (Series) \tag{2.61}$$

$$[C_T] = [T_1][C_{T2}][T_1]^\dagger + [C_{T1}] \quad (Cascaded) \tag{2.62}$$

where the subscripts 1 and 2 represent the two individual two-ports for the cascaded configuration.

Twiss [27], Haus and Adler [28] showed that if a two-port consists only of passive elements, the correlation matrix can be directly calculated from the following relationship

$$[C_Y] = 2kT_0[Y + Y^*] \tag{2.63}$$

$$[C_Z] = 2kT_0[Z + Z^*] \tag{2.64}$$

2.5.3 Noise correlation matrix in terms of noise parameters

It is useful to describe the correlation matrix in terms of the noise parameters F_{min},R_n and y_{opt}, so that the chain correlation matrix can be quickly determined through vendor supplied noise data. This section shows how the chain correlation matrix representation is written in terms of the noise parameters based on the work from [26]. The transformations in Table 2.1 can be used to transform the chain representation to an alternate configuration, depending on the application. From equation (2.53) the chain correlation matrix is written as follows

$$[C_T] = \begin{bmatrix} \overline{v_n v_n^*} & \overline{v_n i_n^*} \\ \overline{v_n^* i_n} & \overline{i_n i_n^*} \end{bmatrix} \tag{2.65}$$

In order to determine the auto-and cross-spectral densities of the chain correlation matrix, consider Figure 2.10, where a noisy amplifier characterised by its ABCD-parameters, is excited

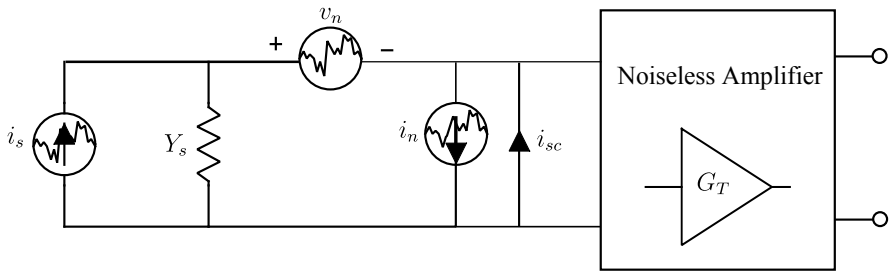


Figure 2.10: Noiseless amplifier excited by a current source with internal noise sources referred to the input

by a source i_s and the noise sources are referred to the input of the amplifier. The relationship between the port noise voltages and Y_s, R_n, Y_c and G_u has already been defined in section 2.4.2. By definition the auto correlation components of the noise voltage can be written in terms of the equivalent noise resistance as follows

$$\overline{v_n^2} = 4kT_0\Delta f R_n \tag{2.66}$$

We also assume as in section 2.4.2 that there exists some correlation between the two internal noise sources generated by the amplifier i_n and v_n which is presented by Y_c. The noise current i_n is divided into two parts shown in equation (2.27) and the auto correlation component of the noise current is calculated as follows

$$\begin{aligned} \overline{i_n^2} &= \overline{(i_{nu} + Y_c v_n)(i_{nu} + Y_c^* v_n)} \\ &= 4kT_0\Delta f G_n + |Y_c|^2\overline{v_n^2} \\ &= 4kT_0\Delta f R_n[\frac{G_n}{R_n} + G_c^2 + B_c^2] \\ &= 4kT_0\Delta f R_n|y_{opt}|^2 \end{aligned} \tag{2.67}$$

The cross-correlation components in terms of the noise parameters are determined by assuming that the noise current can be broken up into two parts, correlated and uncorrelated and the result is

$$\begin{aligned}\overline{v_n i_n^*} &= \overline{v_n(i_{nu} + Y_c v_n)^*} \\ &= Y_c^* \overline{v_n^2} \\ &= (G_c + jB_c)^* 4KT_0\Delta f R_n \end{aligned} \tag{2.68}$$

From equation (2.40) the correlation conductance and suceptance can be written in terms of the minimum noise factor as shown in section 2.4.2. A minimum F could only occur if $B_{opt} = B_c$, it follows that

$$\begin{aligned}\overline{v_n i_n^*} &= 4kT_0\Delta f R_n(\frac{F_{min} - 1}{2R_n} - G_{opt} + jB_{opt}) \\ &= 4kT_0\Delta f \left[\frac{F_{min}}{2} - R_n y_{opt}^*\right] \end{aligned} \tag{2.69}$$

The same approach can be taken to determine the other cross-correlation component $< i_n v_n^* >$ and the result is

$$\begin{aligned}\overline{i_n v_n^*} &= Y_c \overline{v_n^2} \\ &= 4kT_0\Delta f \left[\frac{F_{min} - 1}{2} - R_n y_{opt}\right] \end{aligned} \tag{2.70}$$

Now the auto and cross-spectral densities can be rearranged in matrix form to give the relationship between the noise parameters and the chain correlation matrix,

$$[C_T] = 4kT_0\Delta f \begin{bmatrix} R_n & \frac{F_{min} - 1}{2} - R_n y_{opt}^* \\ \frac{F_{min} - 1}{2} - R_n y_{opt} & R_n |y_{opt}|^2 \end{bmatrix} \tag{2.71}$$

2.6 Multi-port Noise Theory

2.6.1 Noise Analysis of an Admittance N-port

The theory of a noisy two-port can be extended to determine the noise factor and correlation matrix of an N-port network. This derivation is based on work from Rizolli and Lipaparini [29].

Consider the N-port network shown in Figure 2.11, which shows the general admittance matrix with noise sources i_n representing the noise generated at each port by the N-port network. Included in Figure 2.11 are noise sources i_s for each port termination. Starting with the general description of the N-port admittance matrix by writing the voltage and current relationships as follows

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix} = [Y] \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} = \begin{bmatrix} i_{s1} \\ i_{s2} \\ \vdots \\ i_{sN} \end{bmatrix} - \begin{bmatrix} i_{n1} \\ i_{n2} \\ \vdots \\ i_{nN} \end{bmatrix} - \begin{bmatrix} Y_{s1} & 0 & \dots & 0 \\ 0 & \ddots & & \vdots \\ \vdots & & \ddots & \vdots \\ 0 & \dots & 0 & Y_{sN} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} \tag{2.72}$$

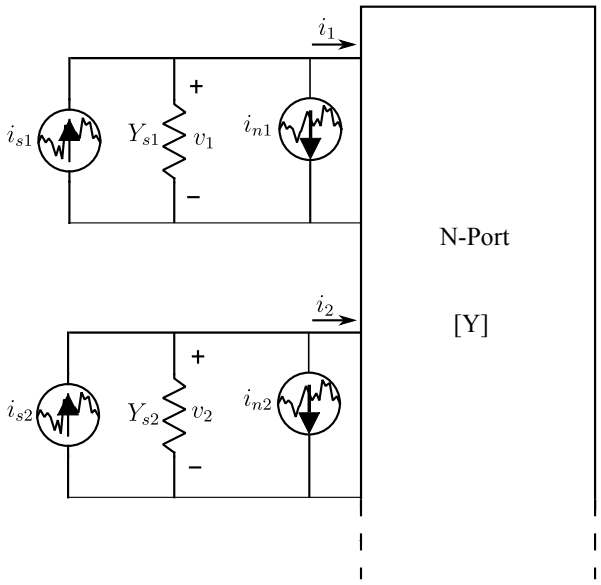


Figure 2.11: N-port passive network

By rearranging the terms of equation (2.72) in compact matrix form the voltages are rewritten in terms of the currents as follows

$$\begin{aligned}[v] &= ([Y] + [Y_s])^{-1}([i_s] - [i_n]) \\ &= [Y_a]^{-1}([i_s] - [i_n])\end{aligned} \tag{2.73}$$

with $[Y_a]$ is the general $[Y]$ matrix augmented with the source matrix $[Y_s]$. Defining $[Z_a]$ as

$$[Z_a] = [Y_a]^{-1} = \begin{bmatrix} [Z_{a1}] \\ [Z_{a2}] \\ \vdots \\ [Z_{aN}] \end{bmatrix} \tag{2.74}$$

where Z_{am} = m-th row of $[Z_a]$, the goal is to calculate the noise factor from port p to q of the N-port. First it is necessary to calculate the noise power delivered to a load termination at port q. Setting Y_{sq} equal to $\frac{1}{Z_L}$, it follows that the voltage at port q is written as follows

$$v_q = [Z_{aq}][i_s] - [Z_{aq}][i_n] \tag{2.75}$$

$$\Rightarrow N_{qo} = \overline{v_q^2} Re[Y_{sq}], \tag{2.76}$$

$$\tag{2.77}$$

with

$$\overline{v_q^2} = \overline{([Z_{aq}][i_s - i_n][i_s - i_n]^\dagger [Z_{aq}]^\dagger)} \tag{2.78}$$

$$= [Z_{aq}]\overline{[i_s - i_n][i_s^* - i_n^*]}[Z_{aq}]^\dagger \tag{2.79}$$

where † represents the Hermitian transpose. It is important to note that all noise generated by the source terminations of each port are assumed to be uncorrelated with each other. Therefore

it is possible to write the following

$$\overline{[i_s - i_n][i_s - i_n]^\dagger} = \overline{[i_s][i_s]^\dagger} + \overline{[i_n][i_n]^\dagger} \tag{2.80}$$

Two correlation matrices are defined, one for the source currents and one for the admittance port currents. The admittance correlation matrix definition remains the same $[C_I] = \overline{[i_n][i_n]}^\dagger$. Assuming that the noise generated by the source terminations are thermal in nature, the source correlation matrix is written as

$$[C_s] = \begin{bmatrix} \overline{i_{s1}i_{s1}^*} & & & \\ & \overline{i_{s2}i_{s2}^*} & & \\ & & \ddots & \\ & & & \overline{i_{sN}i_{sN}^*} \end{bmatrix} \tag{2.81}$$

$$= 4kT_0\Delta f \begin{bmatrix} Re[Y_{s1}] & & & \\ & Re[Y_{s2}] & & \\ & & \ddots & \\ & & & Re[Y_{sN}] \end{bmatrix} \tag{2.82}$$

The output noise power N_q is written in terms of the noise correlation matrices as follows

$$N_q = ([Z_{aq}][C_s][Z_{aq}]^\dagger + [Z_{aq}][C_I][Z_{aq}]^\dagger)Re(Y_{sq}) \tag{2.83}$$

There are two ways to calculate the noise factor at port q. One method includes the noise generated by the other terminations, not just those from port p, which means that each port is terminated by a standard 50 Ω load and the noise generated is also included in the analysis. The other, more general method used by solvers, such as Agilent Design Software (ADS) and AWR microwave office, does not include the noise generated from other port terminations and sets $[C_s] = 0$.

The final step before the noise factor can be calculated is to determine the output noise power from the source of port p N_{po}. The noise generated by this source and that of the network are uncorrelated, therefore the contribution of $[i_n] = 0$, resulting in

$$N_{qo}(source) = [Z_{aq}] \begin{bmatrix} 0 & & & \\ & \ddots & & \\ & & 4kT_0\Delta f Re(Y_{sp}) & \\ & & & 0 \end{bmatrix} [Z_{aq}]^\dagger Re(Y_{sq}) \tag{2.84}$$

$$= |Z_{aqp}|^2 4kT_0\Delta f Re(Y_{sp}) Re(Y_{sq}) \tag{2.85}$$

and the noise factor(F_{qp}) between port p and q becomes

$$F_{qp} = 1 + \frac{[Z_{aq}]([C_s] + [C_I])[Z_{aq}]^\dagger}{|Z_{aqp}|^2 4kT_0\Delta f Re(Y_{sp})} \tag{2.86}$$

2.6.2 Noise Analysis of an N-port containing Active devices

Considering a unique case of an N-port network, where the network is embedded with active devices, it is generally difficult to calculate the noise factor and correlation matrix of the entire network. For this type of problem, the noise correlation matrix for the individual active devices is available from the noise parameters of vendor supplied data, thus it is convenient to follow the derivation by Rizzoli and Lipparini [29].

Figure 2.12 shows a passive noiseless network represented by its admittance matrix which is embedded with m active devices. Each active device is represented by its own correlation matrix $[C_{Jm}]$ and admittance parameters. The noise currents j_1 to j_{2m} resemble the noise generated by the active devices, and the noise sources i_{n1} to $i_{n(2m+n)}$ indicate the noise generated by the passive noiseless network. It is important to note that the port numbering starts at the internal ports and moves outwards towards the external ports as indicated in Figure 2.12.

The voltage and current vectors are subdivided as follows

$$[v] = \begin{bmatrix} v_1 \\ \vdots \\ v_{2m} \\ ---- \\ v_{2m+1} \\ \vdots \\ v_{2m+n} \end{bmatrix} = \begin{bmatrix} [v_d] \\ [v_e] \end{bmatrix} \qquad [i] = \begin{bmatrix} i_1 \\ \vdots \\ i_{2m} \\ ---- \\ i_{2m+1} \\ \vdots \\ i_{2m+n} \end{bmatrix} = \begin{bmatrix} [i_d] \\ [i_e] \end{bmatrix} \tag{2.87}$$

The noise currents of the active devices are arranged from the passive network as follows

$$[N_d] = \begin{bmatrix} i_{n1} \\ \vdots \\ \vdots \\ i_{n(2m)} \end{bmatrix} \qquad [N_e] = \begin{bmatrix} i_{n(2m+1)} \\ \vdots \\ \vdots \\ i_{n(2m+n)} \end{bmatrix} \qquad [J] = \begin{bmatrix} j_1 \\ \vdots \\ \vdots \\ j_{2m} \end{bmatrix} \tag{2.88}$$

From the definition of N-port Y-parameters, we can write the following relationship for the internal and external currents

$$\begin{bmatrix} [i_d] \\ [i_e] \end{bmatrix} - \begin{bmatrix} [N_d] \\ [N_e] \end{bmatrix} = [Y] \begin{bmatrix} [v_d] \\ [v_e] \end{bmatrix} = \begin{bmatrix} [y_{dd}] & [y_{de}] \\ [y_{ed}] & [y_{ee}] \end{bmatrix} \begin{bmatrix} [v_d] \\ [v_e] \end{bmatrix} \tag{2.89}$$

$$\Rightarrow [i_d] = [y_{dd}]\,[v_d] + [y_{de}]\,[v_e] + [N_d] \tag{2.90}$$

$$[i_e] = [y_{ed}]\,[v_d] + [y_{ee}]\,[v_e] + [N_e] \tag{2.91}$$

As each transistor can be treated separately as a two-port, it is possible to write the current

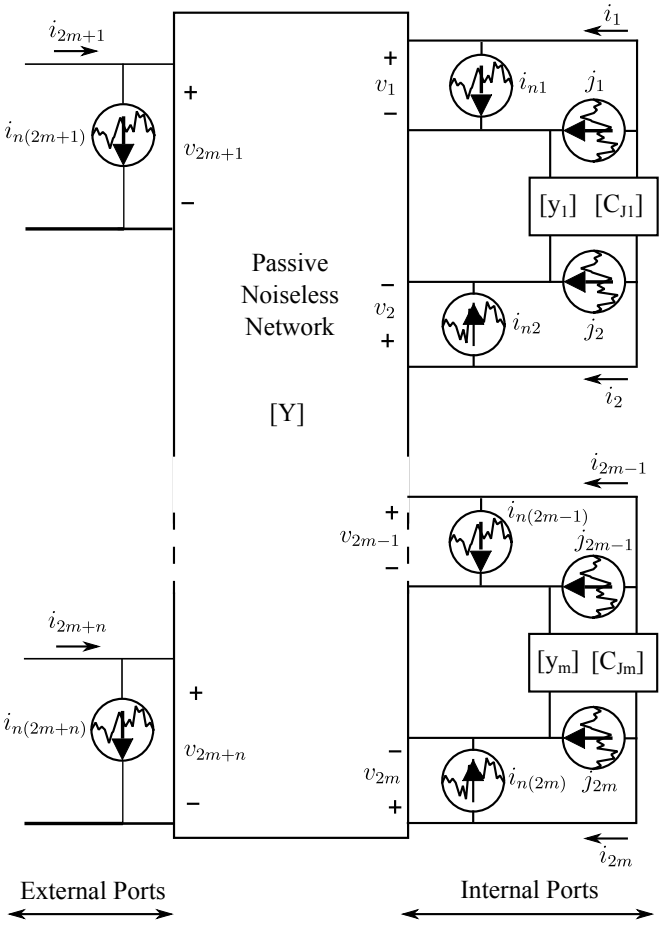


Figure 2.12: N-port passive network

and voltage relationships as follows

$$\begin{bmatrix} -i_1 \\ \vdots \\ \vdots \\ -i_{2m} \end{bmatrix} - \begin{bmatrix} j_1 \\ \vdots \\ \vdots \\ j_{2m} \end{bmatrix} = \begin{bmatrix} [y_1] & & & \\ & [y_2] & & \\ & & \ddots & \\ & & & [y_m]_t \end{bmatrix} \begin{bmatrix} v_1 \\ \vdots \\ \vdots \\ v_{2m} \end{bmatrix} \tag{2.92}$$

$$\Rightarrow [i_d] = -[y_d][v_d] - [J] \tag{2.93}$$

Now that the circuit is subdivided into its active and passive parts, the goal is to derive a new circuit as shown in Figure 2.13. The current and voltage relationships for Figure 2.13 can be written as follows

$$[i_e] - [s] = [Y_L][v_e] \tag{2.94}$$

where $[s]$ is the noise sources at the external ports. Equating equation (2.90) and (2.93) yields the following

$$([y_{dd}] + [y])[v_d] = -[y_{de}][v_e] - [N_d] - [J] \tag{2.95}$$

$$[v_d] = -([y_{dd}] + [y])^{-1}([y_{de}][v_e] + [N_d] + [J]) \tag{2.96}$$

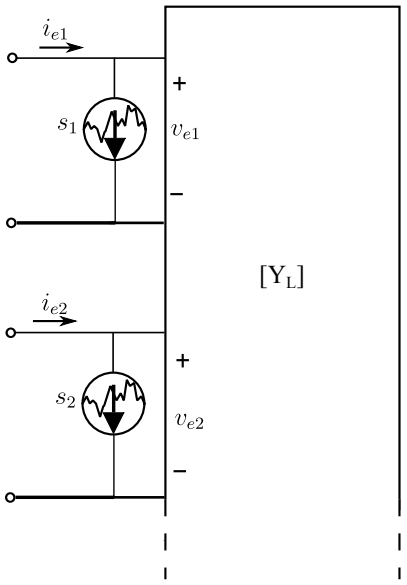


Figure 2.13: N-port passive network

Equation (2.91) are rewritten in the following form

$$\begin{aligned}[i_e] &= [y_{ed}][v_d] + [y_{ee}][v_e] + N_e \\ &= -[y_{ed}]([y_{dd}] + [y])^{-1}([y_{de}][v_e] + [N_d] + [J]) \end{aligned} \tag{2.97}$$

To be more concise the following matrix is defined

$$[H_J] = -[y_{ed}]([y_{dd}] + [y])^{-1} \tag{2.98}$$

and equation (2.97) is written as

$$[i_e] = [H_J][N_d] + [N_e] + [H_J][J] + ([H_J] + [y_{ee}])[v_e] \tag{2.99}$$

resulting in a complete description of the noise currents at the external ports as shown in Figure 2.12. Equation (2.99) is shortened further by defining

$$[H_n] = [H_J|I_n] \tag{2.100}$$

$$\Rightarrow [i_e] = [H_n] \begin{bmatrix} [N_d] \\ [N_e] \end{bmatrix} + [H_J][J] + ([H_J] + [y_{ee}])[v_e] \tag{2.101}$$

where $[I_n]$ is the n-th order identity matrix. The final part of the derivation is to determine $[s]$, where the same $[i_e]$ is calculated for both circuits in Figure 2.12 and 2.13 for any excitation $[v_e]$. If we choose $[v_e] = [0]$, the following relationship between the two circuits can be established

$$[i_e] = [s] \tag{2.102}$$

$$\Rightarrow [H_n][N] + [H_J][J] = [s] \tag{2.103}$$

The final step is to determine the correlation matrix of the entire network which, by definition can be written as

$$[C_s] = \overline{[s][s]^\dagger} \tag{2.104}$$

$$= \overline{([H_N][N] + [H_J][J])([H_N][N] + [H_J][J])^\dagger} \tag{2.105}$$

$$= \overline{[H_N][N][N]^\dagger[H_N]^\dagger} + \overline{[H_N][N][J]^\dagger[H_J]^\dagger}$$

$$+ \overline{[H_J][J][N]^\dagger[H_N]^\dagger} + \overline{[H_J][J][J]^\dagger[H_J]^\dagger} \tag{2.106}$$

Assuming that the noise sources from the active devices $[J]$ and those from the passive network $[N]$ are uncorrelated, allows sets $\overline{[N][J]^\dagger} = \overline{[J][N]^\dagger} = 0$ and for the correlation matrix of the multi-port network to be written as

$$[C_s] = [H_N][C_N][H_N]^\dagger + [H_J][C_J]][H_J]^\dagger \tag{2.107}$$

It is important to note that $[C_J]$ can be written in the following form under the assumption that the noise from different two ports are uncorrelated.

$$[C_J] = \begin{bmatrix} [C_{J1}] & & & \\ & [C_{J2}] & & \\ & & \ddots & \\ & & & [C_{Jm}] \end{bmatrix} \tag{2.108}$$

The last step is to determine the overall admittance matrix of the multi-port,which can be done by setting all the noise sources equal to zero and, from equation (2.101), obtain

$$[i_e] = ([H_J] + [y_{ee}])[v_e] \tag{2.109}$$

$$\Rightarrow [y_L] = [H_J] + [y_{ee}] \tag{2.110}$$

This concludes the basic noise theory that is needed in order to analyse an amplifier circuit. This theory is used extensively in the analysis of the multi-path amplifier discussed in Chapter 6. The theory also gives important insight into the noise analysis of general networks when designing for low noise, using circuit solvers such as ADS or AWR and understanding the software works and its limitations on the software or that of the theoretical analysis.

Chapter 3

Wide-Band Amplifier Design Considerations

There are several factors to consider when designing wide-band LNA's for minimum noise figure. The stability of the amplifier is of great importance, along with amplifying the desired signal equally across the frequency range of interest. This chapter focuses on the basic techniques needed to design a wide-band amplifier, such as basic gain definitions, amplifier stability techniques and negative feedback analysis. The final section shows some important factors that need to be taken into consideration when selecting the appropriate device that is used in the chapters to follow to design wide-band low noise amplifiers.

3.1 Gain Definitions

In RF and microwave amplifier design, an amplifier is characterized according to its S-parameters. Consider the two port amplifier shown in Figure 3.1, with P_{in} and P_L the input and load power

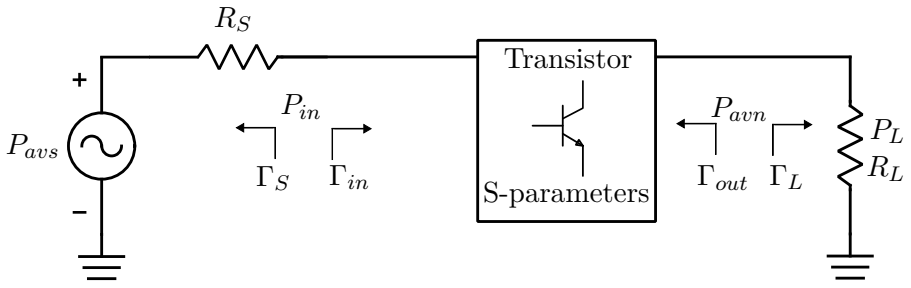


Figure 3.1: Amplifier network showing the different reflection coefficients and Power definitions

respectively, P_{avs} is the available power from the source, P_{avn} is the available power from the network, R_s the source resistance and R_L the load resistance. The three gain definitions of an amplifier are the power gain (G), available power gain (G_A) and the transducer power gain (G_T). Mathematically, these definitions are written as [22]

$$G = \frac{P_L}{P_{in}} = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_L|^2} \tag{3.1}$$

$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)}{(1-|\Gamma_{out}|^2)|1-S_{11}\Gamma_S|^2} \tag{3.2}$$

$$G_T = \frac{P_L}{P_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_S\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2} \tag{3.3}$$

where $\Gamma_S, \Gamma_{in}, \Gamma_L, \Gamma_{out}$ are the reflection coefficients on either side of the amplifier. The main difference between the three definitions are whether they include input and output mismatches between the amplifier and the source or load.

The definition for power gain (G) does not consider whether the source and load are conjugately matched to the input and output of the amplifier. The available power gain (G_A) includes the source mismatches but does not include output mismatches. Thus the definition used in general is G_T, because it includes both the input and output mismatches. A unique situation for the transducer power gain occurs when the input and the output of the amplifier are perfectly matched for zero reflection ($\Gamma_S, \Gamma_L = 0$) and equation (3.3) reduces to [22]

$$G_T = |S_{21}|^2 \tag{3.4}$$

For low noise amplifier design in practice, this is never be the case, since the input is matched for minimum noise instead of maximum power transfer where the criterion could be satisfied. If $S_{12} \approx 0$ then the transducer power gain is redefined as the unilateral transducer power gain G_{TU} and written as [22]

$$G_{TU} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-S_{11}\Gamma_S|^2|1-S_{22}\Gamma_L|^2} \tag{3.5}$$

This non-reciprocal behaviour gives the advantage of designing the input and output network separately since $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$. In wide-band amplifier design this is a useful characteristic since it minimises the iterations of adjusting the input and output matching networks for optimum performance.

3.2 Stability Analysis of an Amplifier

Stability is an important part in any amplifier design. If not done correctly it leads to oscillation instead of amplification. The first step in the design process of an LNA is to stabilize the device. If the designer correctly stabilizes the device, it enables the use of any type of matching network to the input and output of the amplifier. If the device is not stabilized, it limits the creativity of the designer and in most wide band designs it are impossible to add the correct matching topology to operate over a wide bandwidth without oscillation occurring.

3.2.1 Stability Circles

Stability circles are the main method to determine, if an amplifier is stable or unstable with the use of a Smith chart. There are two sets of stability circles, one for the input and one for the

output of the amplifier. According to [22] the equations for the centre point (c_S, c_L) and radius (r_S, r_L) of the source and load stability circles are written as follows

$$c_L = S_{22} - \Delta S_{11}^* \tag{3.6}$$

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \tag{3.7}$$

$$c_S = S_{11} - \Delta S_{22}^* \tag{3.8}$$

$$r_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \tag{3.9}$$

where $\Delta = S_{11}S_{22} - S_{21}S_{12}$.

There are two categories for stability, an amplifier is either unconditionally stable or conditionally stable. In order to determine if an amplifier is conditionally or unconditionally stable both the input and output stability circles need to be plotted as shown in Figure 3.2(a) and (b)

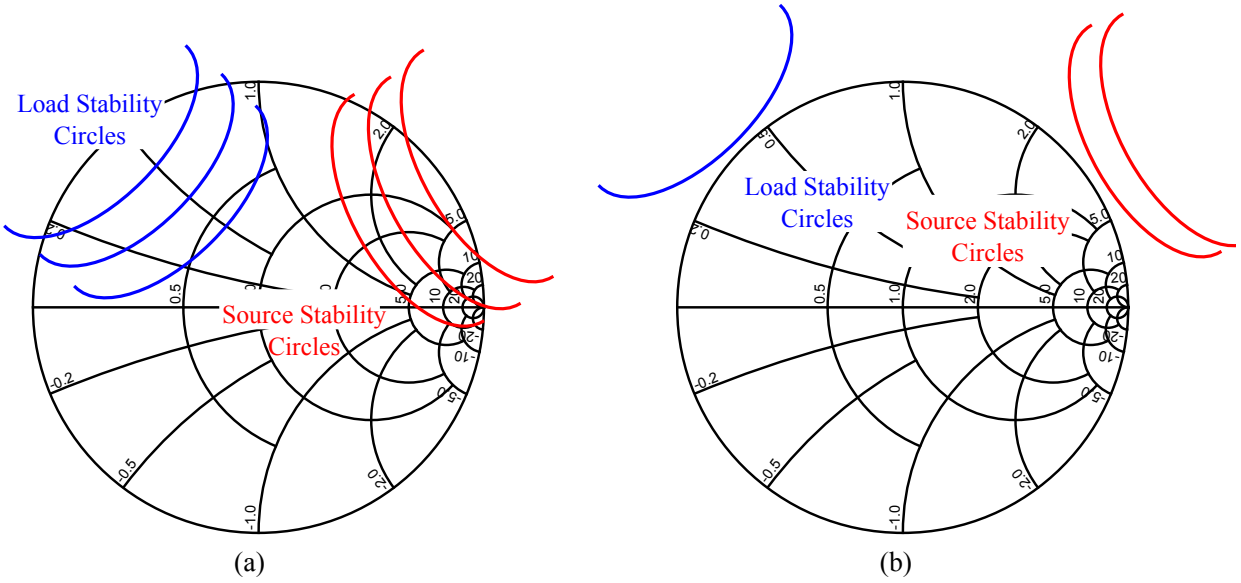
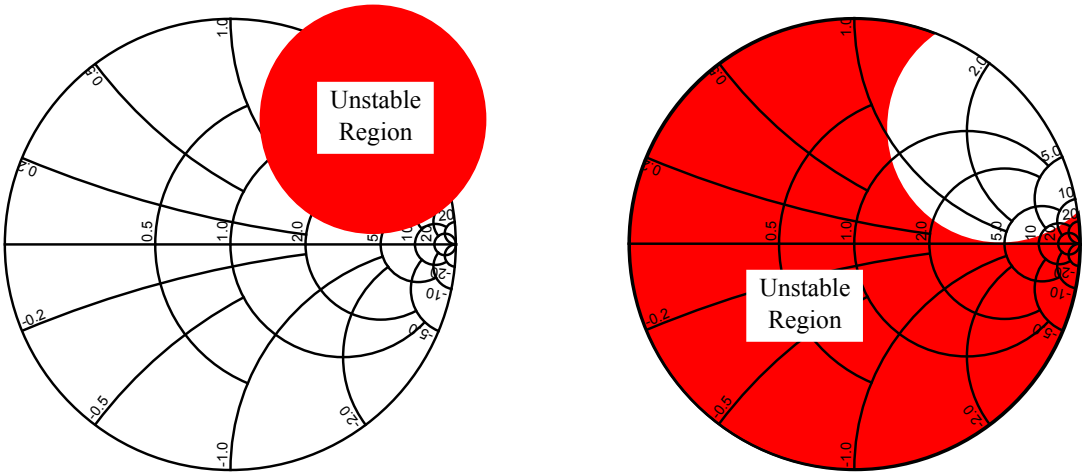


Figure 3.2: (a) Stability circles for a conditional stable device.
(b) Stability circles of an unconditional stable device.

If the stability circles are inside the Smith chart then the active device is conditionally stable and further stabilization methods (see section 3.2.3) are needed in order to make the device unconditionally stable. The second option as shown in Figure 3.2(b) is where both the source and load stability circles are outside the circumference of the smith chart, in which case the active device is unconditionally stable and no further stabilization is needed if the centre is stable.

For a conditionally stable device the stability circles for the source and load need to be plotted according to equations (3.6) to (3.9). In order to determine which side of the stability circle is the stable region, we need to consider $|S_{22}|$ for the source and we need to look at $|S_{11}|$ for the load.

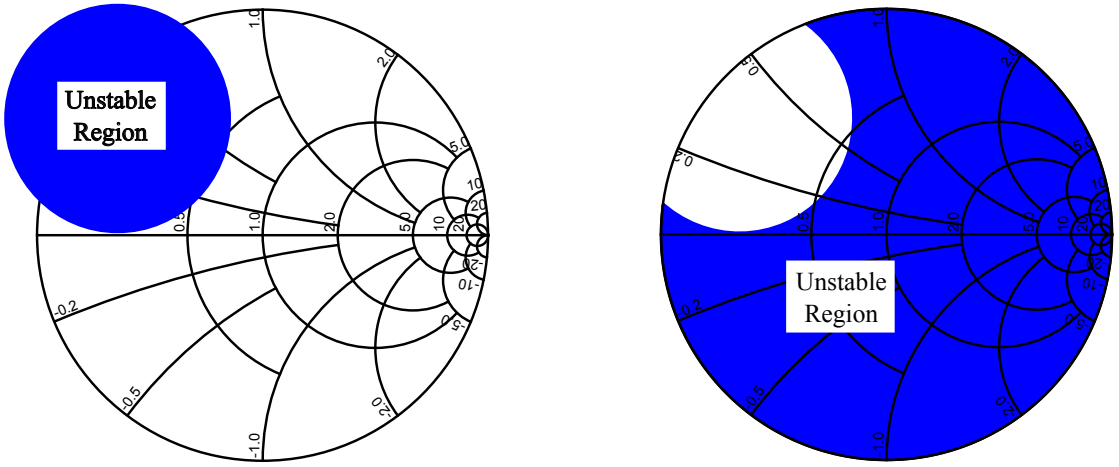


(a) (b)

Figure 3.3: (a) Stability region for source stability circles if $|S_{22}| < 1$
(b) Stability region for source stability circles if $|S_{22}| > 1$.

A source stability circle for a conditionally stable device is plotted in Figure 3.3(a). If $|S_{22}| < 1$ then the unmarked area in white is the stable region of the device as showed in Figure 3.3(a). For the case when $|S_{22}| > 1$, the red area is the unstable region of the device as shown in Figure 3.3(b).

The same method can be applied to the load stability circles, in order to establish which region is stable, $|S_{11}|$ needs to be considered. As an example a hypothetical stability circle is plotted in Figure 3.4(a) and (b), where the regions indicated in blue are unstable.



(a) (b)

Figure 3.4: (a) Stability region for load stability circles if $|S_{11}| < 1$
(b) Stability region for load stability circles if $|S_{11}| > 1$.

3.2.2 $K-\Delta$ and μ Test

The K-Δ and μ tests give a fast and effective way to determine if the amplifier is conditionally or unconditionally stable without the need to plot the stability circles first. The criteria for the K-Δ test is as follows [22]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{3.10}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{3.11}$$

If either criterion (3.10) or (3.11) is not satisfied, the amplifier is conditionally stable and the stability circles need to plotted to determine the stability regions as showed in section 3.2.1.

The μ-test can simply be defined as [22]

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{3.12}$$

For $\mu > 1$, the amplifier is unconditionally stable and a larger μ indicates greater stability. Thus the process to establish the stability of a transistor are as follows, first, use the $K-\Delta$ or μ test to determine if the transistor is unconditionally stable or conditionally stable. If the transistor is conditionally stable, the stability regions need to be established and some of the stabilization methods in section 3.2.3 can be used to stabilise the device.

3.2.3 Stabilization Methods

As mentioned earlier it is important to stabilize a device to enable the designer to add any matching topology to the input and out of the network. In this section the methods on how to add stabilization networks to the input and output of the active device are discussed. There are several configurations when adding a stability element to an amplifier as shown in Figure 3.5 and Figure 3.7

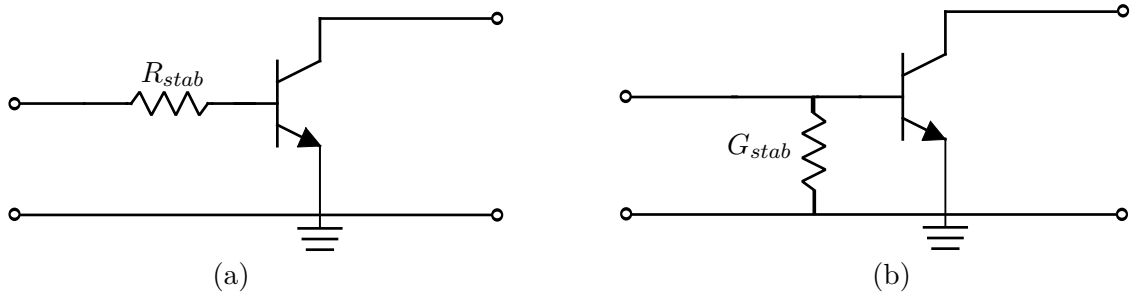


Figure 3.5: (a) Series stability network at the input of the amplifier
(b) Shunt stability network at the input of the amplifier.

The process to determine the value of the stabilization resistor R_{stab} is done graphically by using the Smith chart and examining the stability circles. If the circles are close to the zero impedance part of the Smith chart, as shown in Figure 3.6(a), it is simpler to add a series resistor at the input of the amplifier (see Figure 3.5(a)). The value of R_{stab} can be determined by using the

impedance circles indicated by the dashed magenta circle and reading off the normalised value for R_{stab}. Using this method the value of R_{stab} is more practical in the sense that it decreases the gain of the amplifier by a smaller amount.

For a different case where the source stability circles fill the open circuit part of the smith chart(dominate the right part), it is preferred to add a shunt stability resistor (see Figure 3.5 (b)) at the input of the amplifier. The value for G_{stab} is calculated by using the admittance circles and reading off the value of the normalised admittance G_{stab} as indicated in Figure 3.6(b) by the dashed magenta circle.

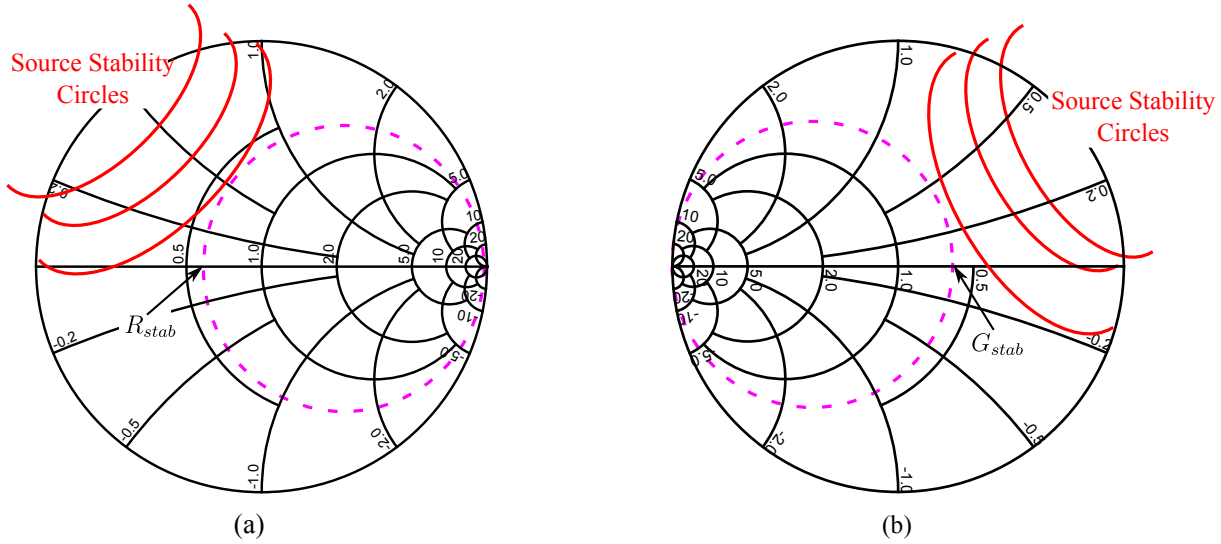


Figure 3.6: (a) Calculation of series stability resistor R_{stab}
(b) Calculation of shunt stability resistor G_{stab}.

The minimum value of R_{stab} is the value obtained from the dotted magenta circle that almost touches the closest stability circle. If more stability is needed the value of R_{stab} can be increased for the series stabilization or decreased for the parallel stabilization topology. The disadvantage of adding more stability to the amplifier is that the gain of the amplifier decreases and the designer is faced with a decision to determine how much stabilization is needed.

A good starting point is to start with the minimum amount of stabilization close to the first stability circle and then add a small margin of stability of about 5 % to ensure that the device is stable and still be able to achieve a high gain level [30]. If after adding the rest of the configurations in the design process such as matching networks, feedback, biasing etc. the circuit becomes unstable, the stability network can be adjusted slightly to re-enforce the stability (make the amplifier stable again) which should have the smallest effect on the other configurations.

Adding only a resistor in series or in parallel at the input or output of the amplifier, attenuates the gain equally across the entire frequency range. In certain cases attenuating the gain across the entire bandwidth is not desired because the device might already be stable in that frequency

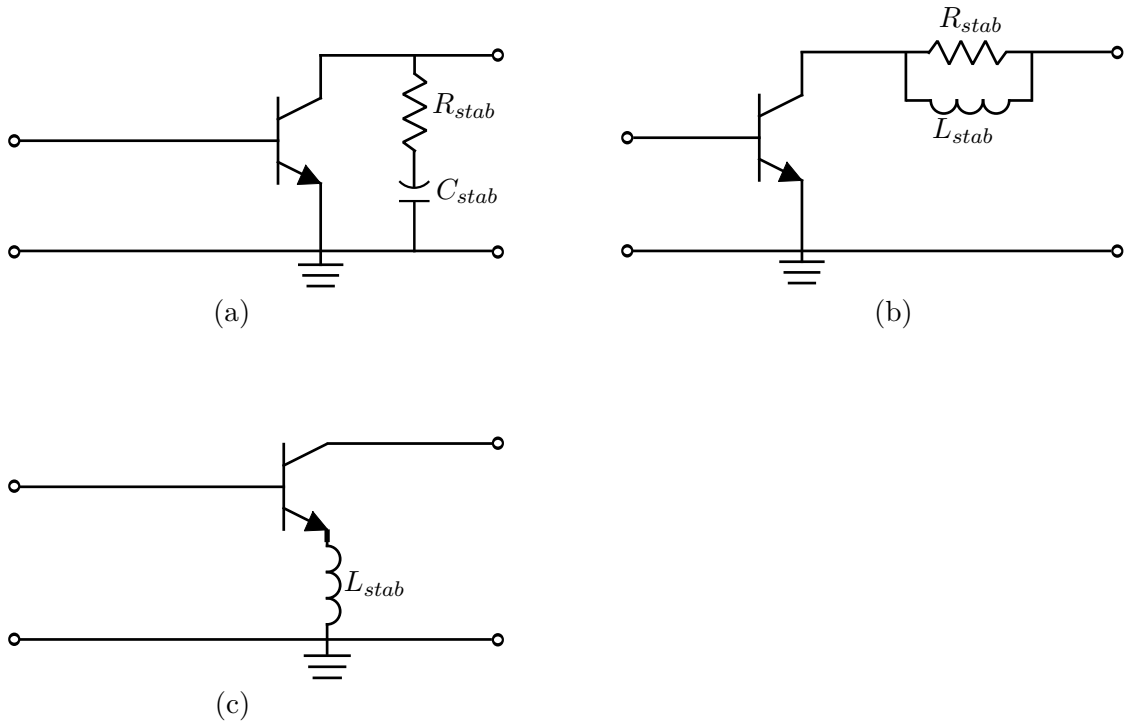


Figure 3.7: Different Stability Configurations:(a)Shunt Resistor in series with Capacitor (b) Series stability resistor with parallel inductor (c) Series inductor connected to emitter port.

range. An inductor in parallel with a series resistor or a capacitor in series with a shunt resistor as shown in Figure 3.7(a) and (b) can help give the desired response of only sacrificing gain at certain frequencies. The final values for the capacitors and inductors are determined with simulation software such as ADS and AWR where the parasitic effects of these components can be taken into consideration which may affect the cutoff frequency of the specific components.

Another technique which can be used to stabilize the transistor at lower frequencies involves adding an inductor L_{stab} as shown in Figure 3.7(c). The disadvantage of this technique is that it degrades the stability at higher frequencies and in most cases it is used in conjunction with the other techniques to enable stability over a wide band. This technique is very sensitive and the designer must take great care in modelling all the effects of the PCB to prevent oscillation [30].

Example: Stabilization of a BFP740 transistor from 0 - 10 GHz

For this example an HBT-BFP740 transistor from Infineon is selected and biased at $V_{ce} = 3$ V and $I_c = 6$ mA. The goal is to stabilize the transistor and achieve a gain of 15 dB at 500 MHz. Consider the complete stabilized amplifier in Figure 3.8, where the stabilization process is done in separate stages as follows.

The transistor is simulated with no stability network attached and the results of the μ-stability factor is shown in Figure 3.9. The blue line shows that the transistor is potentially unstable up until 5.8 GHz, therefore the focus should be on the low frequencies. Adding an inductor in series at the emitter port of the transistor, improves the low frequency stability without sacrificing too

much gain. A value of 0.62 nH is added at the emitter and the result is shown in Figure 3.9(a) by the magenta line.

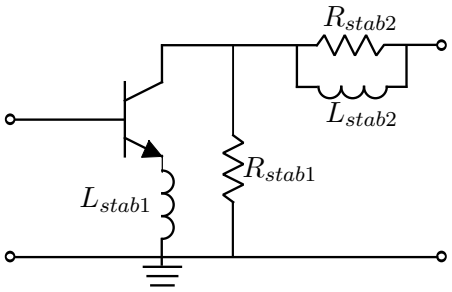


Figure 3.8: BFP740 transistor with stabilization network

As seen in Figure 3.9(a) the low frequency stability is improved but the amplifier is unstable at the higher frequencies. This indicates that, at high frequencies, it is not advisable to add a series inductor at the emitter as this could lead to instability. A shunt resistor is added at the output along with the series inductor by using the conductance circle technique as described in section 3.2.1. The value for $R_{stab1} = 105\ \Omega$ decreases the gain slightly but the stable at the lower frequencies as indicated by the black line in Figure 3.9(a) and (b).

The final step is to stabilize the high frequencies, which is done by adding a series resistor along with an inductor in parallel in order to decrease the gain at the higher frequencies, where necessary. Again to calculate the value of R_{stab2} the impedance circle method is used and the value for $R_{stab2} = 170\ \Omega$ is established. The inductor L_{stab2} is tuned to 6 nH, where the high frequencies is stabilized as shown by th red line in Figure 3.9(a). The gain of the amplifier is 16 dB at 500 MHz indicated by the red line in Figure3.9(b) which achieves the desired specification.

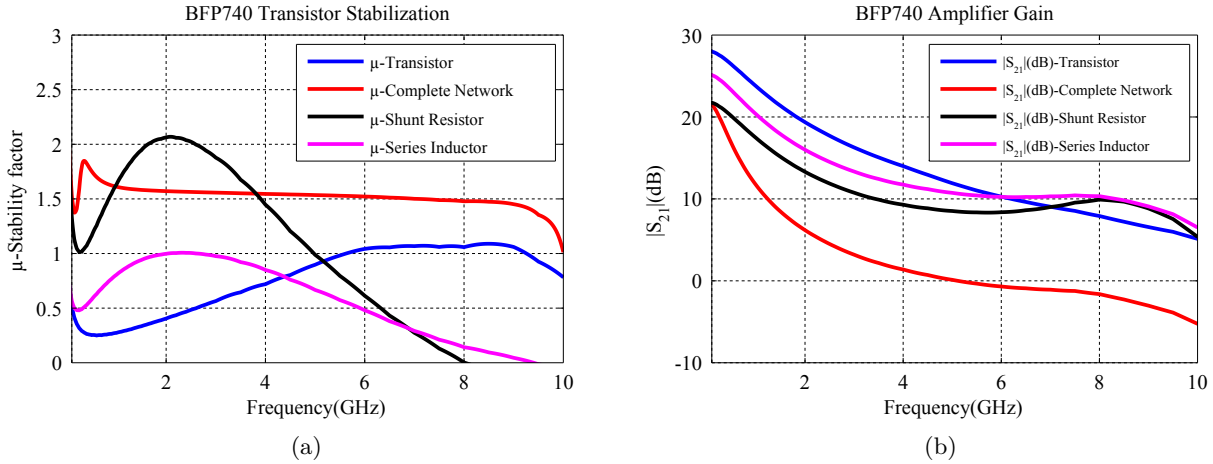


Figure 3.9: Simulation Results of (a) Stability factor μ (b) Gain

3.3 Negative-Feedback

Feedback is widely used in engineering to enforce control over a certain parameter in a system, which is accomplished by feeding the output back to the input as shown in Figure 3.10. Depending on the application, the signal could either be added to or subtracted from the input to achieve the desired response.

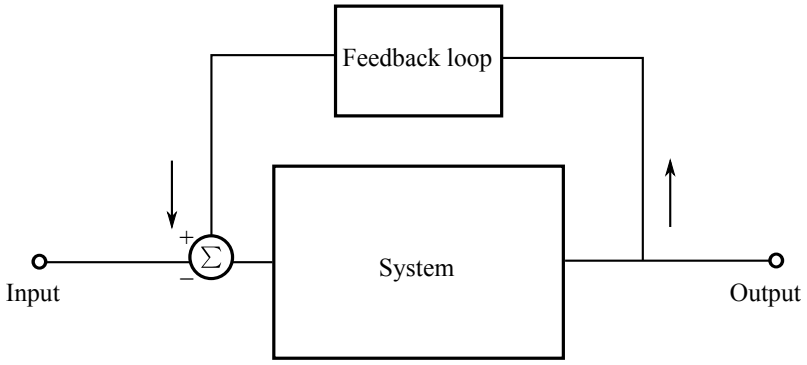


Figure 3.10: General feedback concept

In amplifier applications negative-feedback is used to control the gain of the amplifier to achieve a flat gain response over very wide bandwidths. This is accomplished by attenuating the input signal at the lower frequencies where the gain level is very high. There are other benefits of using negative-feedback than just controlling the gain level, for example, if the feedback network is designed correctly it can improve DC and RF stability and reduce temperature component tolerances [30]. One of the disadvantages of using feedback is that the noise figure of the overall system is degraded and a thorough analysis of this affect is shown later in an example.

There are two types of configurations used in negative feedback design, the first consists of series feedback where a resistor is added to the emitter port of the transistor. The other configuration makes use of parallel feedback, where a resistor is added between the base and collector of the transistor [30, 24]. Both of the configurations are showed in Figure 3.11

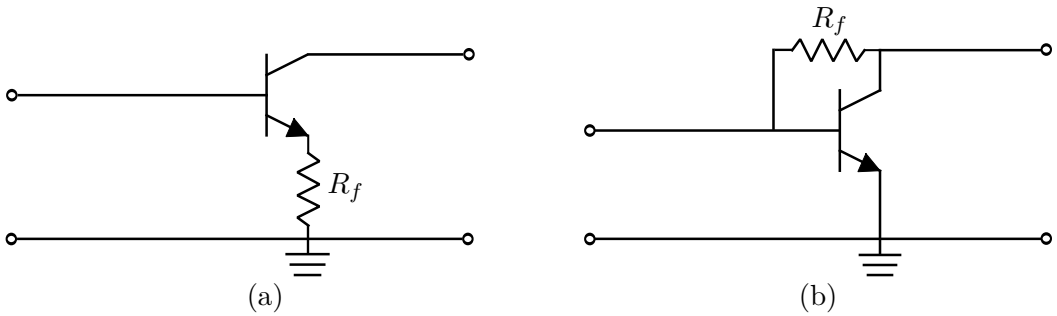


Figure 3.11: (a) Series feedback configuration
(b) Parallel feedback configuration.

The common-emitter configuration is used because there is a 180° phase shift between the output and input ports. Other configuration types such as common-base and common-collector do

not work since, the input and output are in phase with each other [30].

According to [30], as the operation frequency increases the parasitic effects of the active device cause an additional phase shift in the signal. This extra shift in the output phase can cause the emitter configuration to give positive feedback, resulting in instability or oscillation. A phasor-diagram indicating the change in the magnitude and phase of the output voltage V_{out} as the frequency is swept from DC to f_3 is shown in Figure 3.12. If the phase moves beyond the 90° point, indicated by the red doted line in Figure 3.12 the positive feedback can start to create instability in the amplifier.

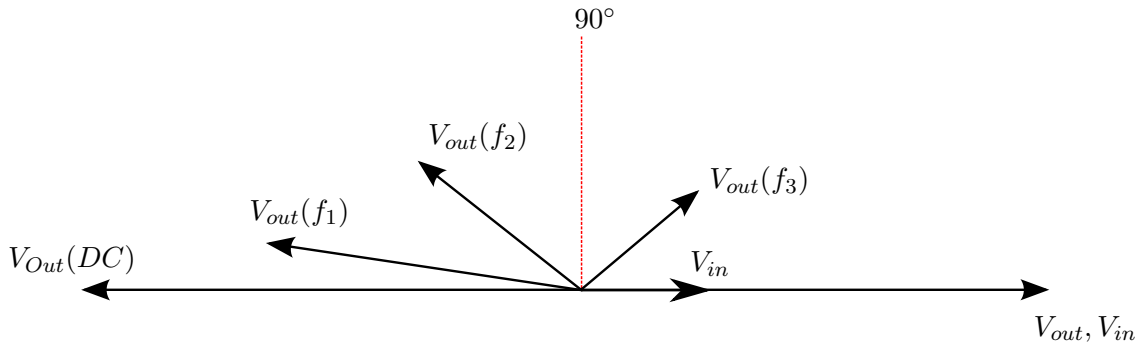


Figure 3.12: Phasor-diagram showing the relationship between V_{in} and V_{out} as the frequency increases in a clockwise direction

In order to determine the design equations for the resistors R_f shown in Figure 3.11, we have to consider the $\pi - model$ of the BJT shown in Figure 3.13(a)

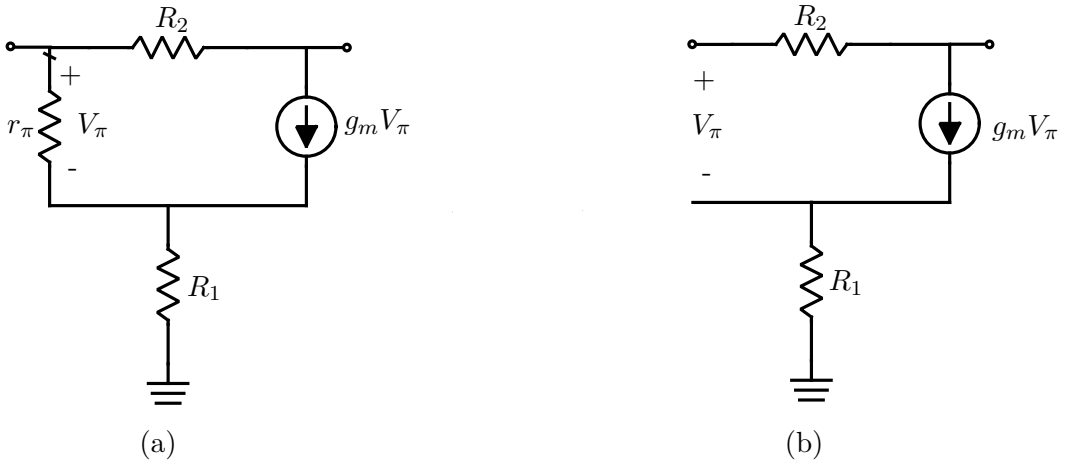


Figure 3.13: (a)$\pi-$model of Feedback amplifier (b)Equivalent model of feedback amplifier assuming that $(r_\pi)(1 + g_m R_2) >> R_1$.

If we assume that $r_\pi(1 + g_m R_2) >> R_1$, this leads to the equivalent circuit shown in Figure 3.13(b). The Y-parameters for this circuit are written as follows

$$[Y] = \begin{bmatrix} \frac{1}{R_2} & -\frac{1}{R_2} \\ \left(\frac{g_m}{1+g_m R_1}\right) & \frac{1}{R_2} \end{bmatrix} \tag{3.13}$$

Using Table 4.2 in [22] to convert from $[Y]$ to [S] parameters, the following results are obtained

$$S_{11} = S_{22} = \frac{1}{D}\left(1 - \frac{g_m Z_0^2}{R_2(1+g_m R_1)}\right) \tag{3.14}$$

$$S_{21} = \frac{1}{D}\left(\frac{-2g_m Z_0}{1+g_m R_1} + \frac{2Z_0}{R_2}\right) \tag{3.15}$$

$$S_{12} = \frac{2Z_0}{DR_2} \tag{3.16}$$

where,

$$D = 1 + \frac{2Z_0}{R_2} + \frac{g_m Z_0^2}{R_2(1+g_m R_1)} \tag{3.17}$$

Assuming that the input and output port are matched ($S_{11} = S_{22} = 0$), then from equation (3.14) the following relationship is written

$$1 + g_m R_1 = \frac{g_m Z_0^2}{R_2} \tag{3.18}$$

$$\Rightarrow R_1 = \frac{Z_0^2}{R_2} - \frac{1}{g_m} \tag{3.19}$$

Substituting equation (3.19) into (3.15) and (3.16), yields the following relationship

$$S_{21} = \frac{Z_0 - R_2}{Z_0} \tag{3.20}$$

$$S_{12} = \frac{Z_0}{R_2 + Z_0} \tag{3.21}$$

Equation (3.20) shows that in order to establish a flat gain response the only dependent variable is the resistor R_2. The shunt-feedback configuration can be analysed by setting $R_1 = 0$ in (3.14)–(3.16). For a BJT it is important to remember that the condition $((r_\pi)(1+g_m R_2) >> R_1)$ must also be satisfied, otherwise the resistor R_1 is needed. If $R_1 = 0$, the feedback design equation is written as follows [24]

$$R_2 = Z_0(1 - |S_{21}|) \tag{3.22}$$

The design equation used to calculate the value of R_2 is only valid at lower frequencies since the parasitic effects of the transistor and PCB have not been taken into consideration. In practice, at RF frequencies an inductor can be added in series with the feedback resistor to help improve the gain flatness and stability by adding extra phase in the feedback loop to keep the device stable. Mathematically the value for the feedback inductor can be calculated as follows [24]

$$L_f = \frac{R_2}{\omega_c} \tag{3.23}$$

where w_c is the cut-off frequency of the desired gain response and R_2 is the feedback resistor. In low noise applications it is preferable to omit the series resistor R_1 in the feedback design because it increases the noise figure of the device and could cause instability if there is some parasitic effects not perfectly modelled in the series feedback loop. An example showing all the factors in play when designing for a flat gain response and with the goal of achieving a certain noise figure are shown next.

Example: Negative Feedback Design Considerations

Consider the feedback amplifier shown in Figure 3.14, where the goal is to demonstrate how to add the parallel feedback network to an amplifier for low noise design. The design specifications for the feedback network are as follows

- NF = 1.2 dB
- Gain = 15 dB
- Operation bandwidth: 250 MHz - 1.25 GHz

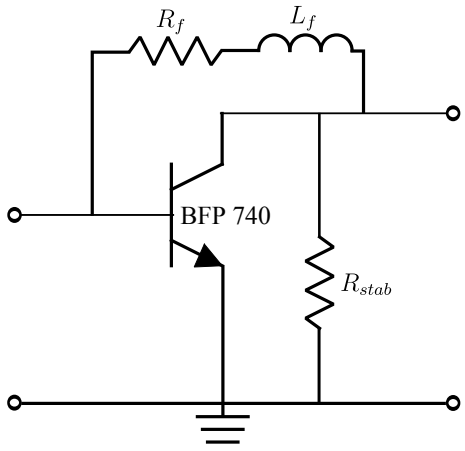


Figure 3.14: Feedback amplifier with stabilization transistor

The Infineon BFP740 transistor is chosen and biased at $V_{ce} = 3$ V and $I_c = 6$ mA for minimum noise operation as shown in the data sheet [31]. Normally the first step in the design procedure is to add the stability network. This is done by plotting the source and load stability circles and using the admittance and impedance circles on the smith chart to calculate the value for the stability resistor $R_{stab} = 25\ \Omega$, as discussed in section 3.2.

A shunt resistor is selected for stability since it minimizes the noise added to the amplifier, but adding just a single resistor at the output in this case does not stabilise the device. A good approach before adding extra stability networks is to add the feedback network to the design. Adding the negative feedback network influences the stability of the device and it minimizes the amount of iterations needed in order to stabilise the device.

The starting value for R_f and L_f are determined from equation (3.22) and (3.23) as follows

$$R_f = 50(1 + 5.623) = 331.17\ \Omega$$
$$L_f = \frac{331}{2\pi(1250\ \text{MHz})} = 42\ \text{nH}$$

After adding the feedback network to the amplifier as shown in Figure 3.14 and simulating the circuit in AWR. The results of the simulation can be viewed in Figure 3.15. The gain level of the feedback network, indicated by the blue line in Figure 3.15(a) decreases quite significantly

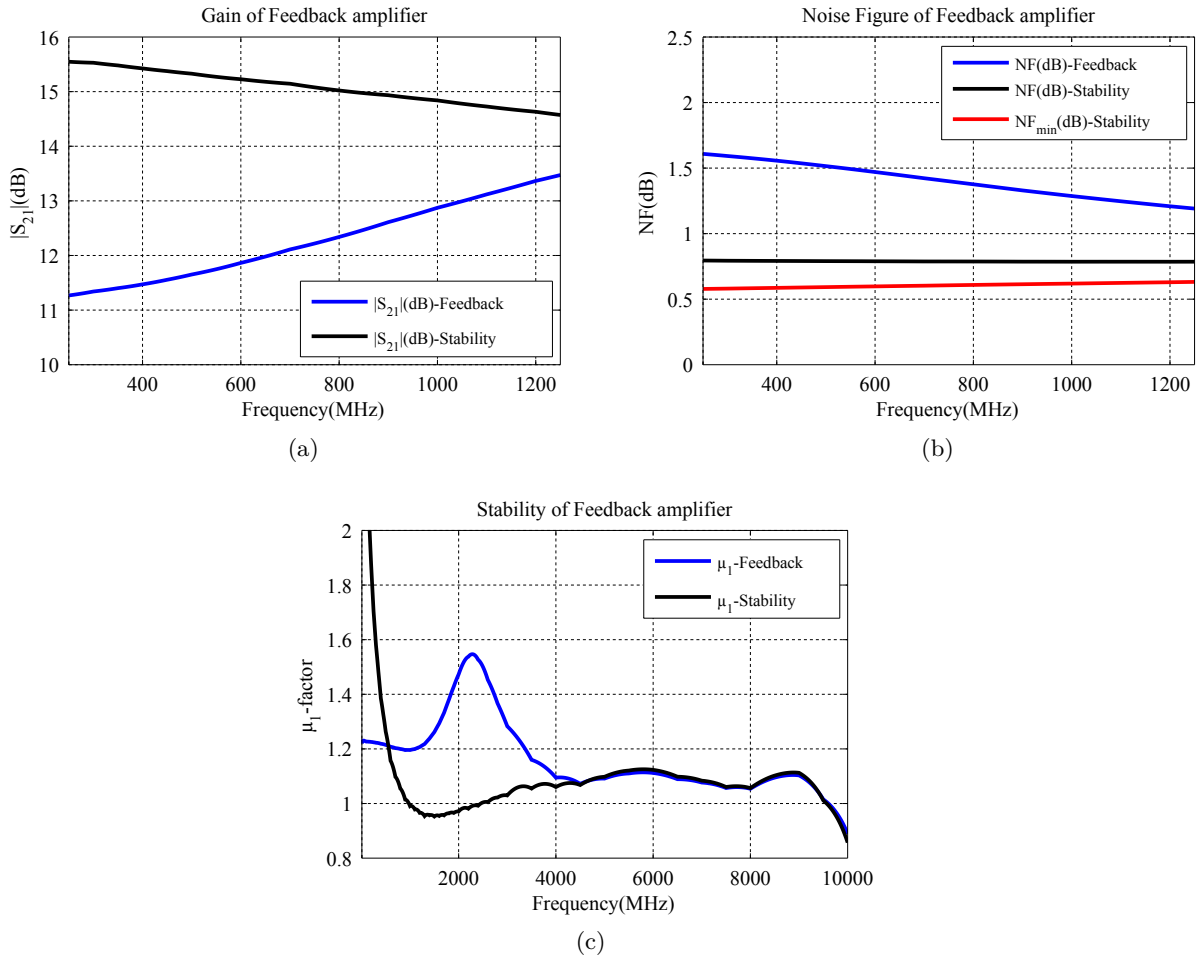


Figure 3.15: Response of starting values for R_f compared to Stability network with no feedback: (a) Gain (b) Noise (c) Stability

to 11 dB at the lower frequencies. In comparison, the black line only decreased about 1 dB across the frequency range of interest when only the stability resistor is at the output. The noise figure of the feedback network also increased to above 1.5 dB, indicated by the blue line in Figure 3.15(b). The only improvement is in the stability of the device, where the device is now stable at the lower frequencies, shown by the blue line in Figure 3.15(c).

The reason for the gain mismatch is that the feedback resistor calculation did not include the feedback inductor to help with the stability improvements. Another reason for the increase in noise figure is that the flat gain calculations assume a perfect input and output power match which is not the case for LNA designs. A solution to improve the noise figure and simultaneously obtain the flat gain response can be achieved by decreasing the impact of the feedback loop by means of increasing R_f and L_f.

In order to demonstrate how the gain, noise figure and stability is influenced by the feedback loop's R_f and L_f, the value of R_f is swept from 200 Ω to 800 Ω while maintaining the value of L_f at 18 nH. The results are shown in Figure 3.16(a) and (b). If the feedback is increased by decreasing the resistor R_f, the gain at the lower frequencies decreases, as indicated by the blue

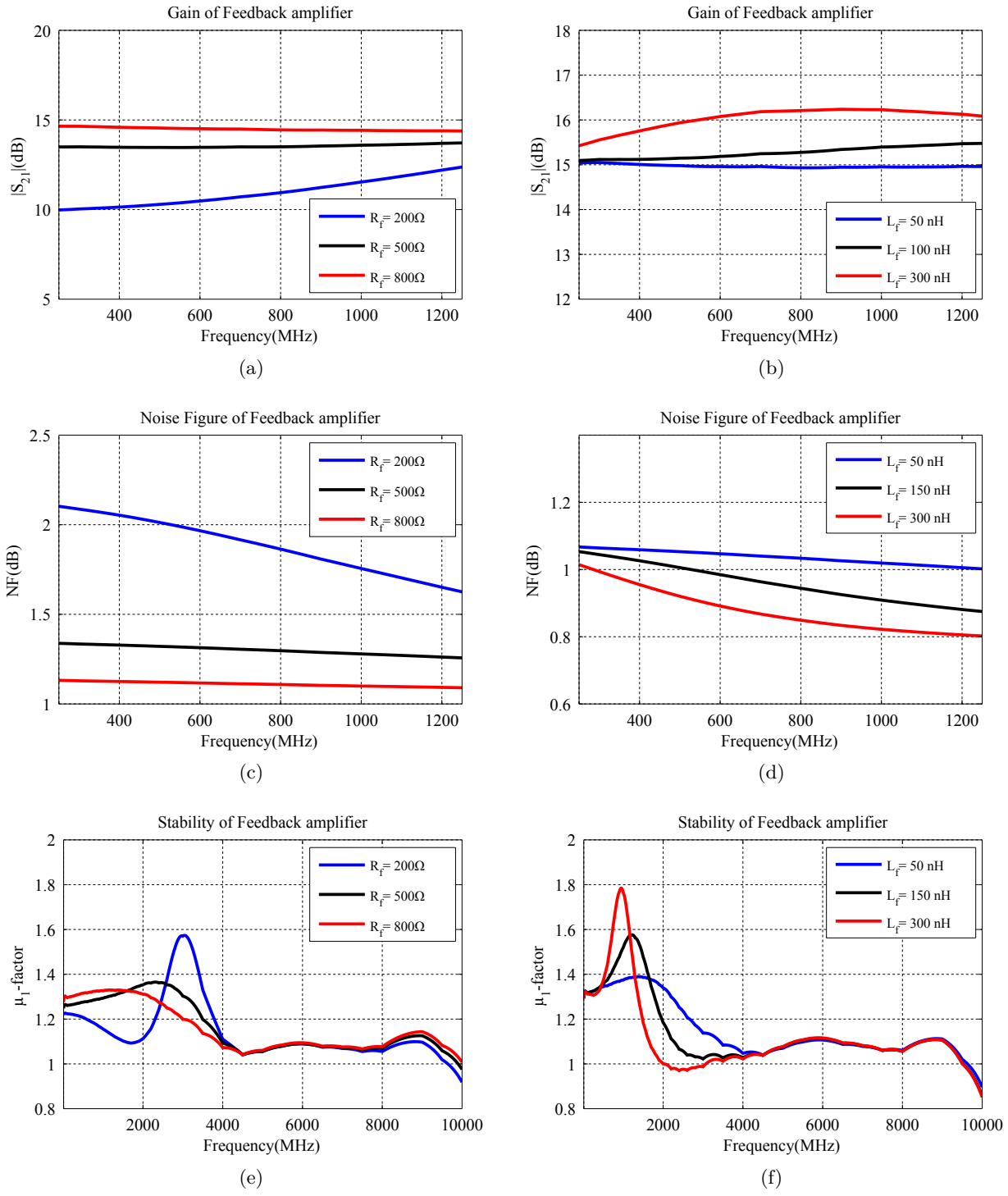


Figure 3.16: Response of the Feedback amplifier by adjusting the feedback network (a) Gain R_f (b) Gain L_f (c) Noise Figure R_f (d) Noise Figure L_f (e) Stability R_f (f) Stability L_f

line in Figure 3.16(a). If the feedback is decreased by increasing R_f then the gain increases, as indicated by the red and black lines in Figure 3.16(a). The noise figure at the lower frequencies also improves, if less feedback is used by increasing the value of R_f as shown in Figure 3.16(c). The stability of the device is mainly dependent on the stability resistor R_{stab} and the value of the feedback inductor. As shown in Figure 3.16(e)the effect on the stability is minimal if R_f is varied quite significantly as the device remains stable across the frequency range and only

becomes potentially unstable close to 10 GHz.

The influence of the inductor is simulated by keeping the resistor $R_f = 960\ \Omega$ and sweeping the inductor value from 50 nH to 300 nH. The gain of the amplifier is affected at the higher frequencies as shown in Figure 3.16(b) by the blue, black and red lines. If the value of L_f is increased too much it affects the slope of the gain to have a positive incline. The noise figure is also dependent on the amount of feedback used, if the feedback is decreased by increasing L_f the noise figure at the higher frequencies decreases, as shown in Figure 3.16(d).

Adjusting the stability of the device is accomplished by decreasing the feedback and increasing L_f as shown in Figure 3.16(f). Again the stability is mostly dependant on the stability resistor R_{stab} but improvements can be made by adjusting L_f. The final optimal values for R_f is equal to 960 Ω, and the value for L_f is equal to 180 nH. The stability resistor is adjusted to 32 Ω. It is clear that a compromise must be made between the noise figure and flat gain response if negative feedback is used. The same trade off is demonstrated later when this technique is used in chapter 5 to design a wide-band LNA.

3.4 Transistor selection

Low noise amplifiers are an important component in a communication system but choosing a transistor for optimum wide-band, low noise performance is a difficult task. The current standard is transistor technologies such as Bipolar Junction Transistors(BJTs) and Field Effect Transistors(FETs). Heterojunction Bipolar Transistor (HBT) is an extension of the BJT technology and operate on the same principle. The main difference is in the conducting material used in the transistor, where a HBT uses SiGe for the conducting layers for a BJT. HEMT technologies is the advancement in FET technology and possesses excellent low noise characteristics as well as the ability to be manufactured in MMIC [6]. The disadvantage as mentioned in chapter 1 is that the HEMT technology does not meet the power consumption abilities of the SKA.

A comparison between the gain and noise figure of the two technologies can be viewed in Table 3.1

FET Technology:			
Product no.	Gain(dB)	NF(dB)	Technology
ATF-38143	16	0.4	HEMT
ATF-35143	18	0.4	HEMT
ATF-531P8	20	0.6	P-HEMT
BJT Technology:			
Product no.	Gain(dB)	NF(dB)	Technology
BFP842ESD	23.5	0.4	HBT
BFP740ESD	27	0.5	HBT
BFP640ESD	24	0.65	HBT

Table 3.1: Comparison of different transistor technologies [32, 33]

As shown in Table 3.1 the main difference in the technologies is the maximum gain level that can be achieved by a single transistor. For the purpose of this project the goal is to develop a single stage LNA which incorporates feedback and matching networks as shown in chapter 5. For a limited amount of stages (due to power consumption reasons), the first stage should have significant gain characteristics as well as low noise performance. This is why the HBT technology was chosen to be investigated, since it provides excellent high gain performance and excellent low noise figure over the operation bandwidth from 350 MHz to 1200 MHz.

Chapter 4

Wide-Band Matching Theory

There are several reasons why impedance matching is needed in a communication system. The first and one of the most important reasons would be to obtain maximum power transfer between the source and the load. This is achieved by minimizing the reflections between the source and load while simultaneously decreasing the power loss in the system.

In the case of LNA's, however, maximum power gain (or minimum reflection) is not the primary concern at the input of the amplifier, as the LNA has a specific noise impedance it needs to be matched to in order to achieve a minimum noise figure. Achieving a low noise figure improves the signal to noise ratio of the system and set the benchmark for the sensitivity of the SKA.

There are certain limitations that occur when a wide-band matched is desired. This was investigated by Bode and Fano [34]. A criterion was developed, which states the absolute limit a matching network can achieve across a certain bandwidth, given that the characteristics of the load are known.

This chapter covers the fundamentals of impedance matching. Several techniques for matching different types load impedances, for both real impedances (resistive values at the out put ports) and complex impedances (a real load with inductive or capacitive characteristic). The examples focus on lumped element circuits, but the theory could easily be extended to different topologies depending on the frequency range of operation.

4.1 The Fundamentals of Impedance Matching

It is known that maximum power transfer will occur between a source and a load, when the load is conjugately matched to the source [35], as in (4.1)

$$Z_L = Z_S^* \tag{4.1}$$

with Z_L the load impedance and Z_S the source impedance. Equation (4.1) is explained graphically as indicated in Figure 4.1

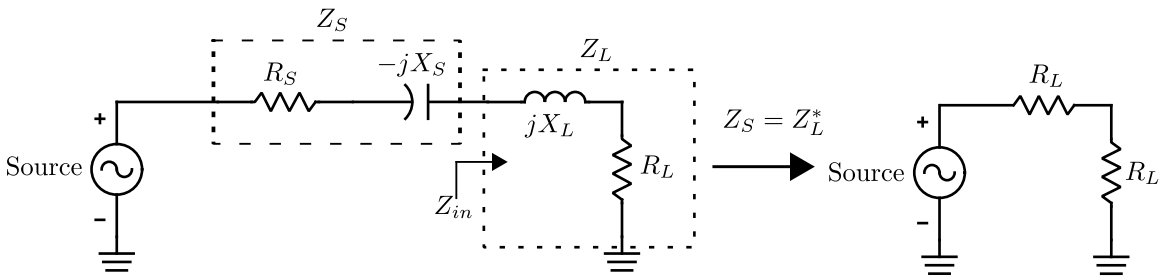


Figure 4.1: Impedance matching procedure

As X_L and R_L are often frequency dependent, a perfect match can only be achieved at discrete frequency points. In the next section the limitations of broadband matching will be investigated.

4.2 Limitations of Wide-band Matching

The limitations of broad-band matching was first described mathematically by Bode and Fano [34]. This criterion sets the benchmark for ideal matching networks, it allows the comparison of different types of matching networks and gives an optimum reflection coefficient for the selected load configuration. The Bode-Fano Criterion for a series R-L load as shown in Figure 4.2 is written as

$$\int_0^\infty ln\frac{1}{|\Gamma(\omega)|}d\omega < \frac{\pi R_L}{L} \tag{4.2}$$

where $\Gamma(\omega)$ is the reflection coefficient as seen from the input port and R_L is the real part of the load impedance and L is the load inductance. It is useful for the discussion later to define the quality factor Q of the load as follows [22]

$$Q = \frac{\text{average energy stored}}{\text{energy loss/second}} = \frac{\omega L}{R_L} \tag{4.3}$$

where ω is the angular frequency in rad/s. As indicated by equation (4.3), if a series R-L load is more inductive the Q increases and it decreases if R_L increases.

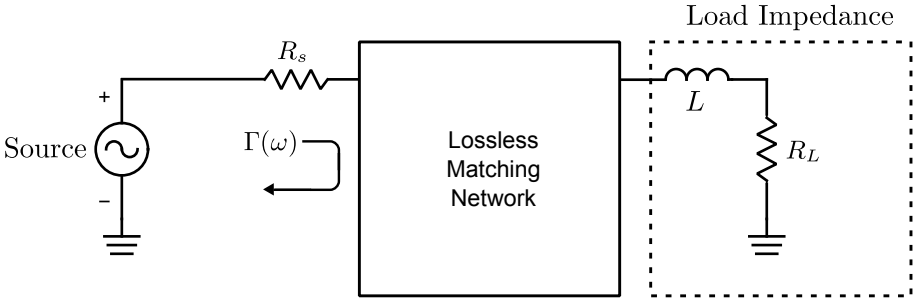


Figure 4.2: Circuit for the Bode-Fano criterion for an R-L load with a lossless matching network with lumped components

Equation (4.2) indicates that if L increases the bandwidth becomes smaller to maintain the same reflection coefficient. This means that if the Q of the load increases, the only way to achieve

the same bandwidth is to sacrifice matching performance and have a bigger reflection coefficient.

In order to demonstrate the effect that the change in Q-factor has on the reflection coefficient, two matching networks were designed over a fixed bandwidth from 400 MHz to 900 MHz with the complex matching technique described in section 4.4. The load for matching network 1 was $Z_L = 100\ \Omega + 37.7\ \Omega$ and for matching network 2 was $Z_L = 100\ \Omega + 75\ \Omega$. A third order Chebychev network was used for each matching network as showed in Figure 4.3, and the values

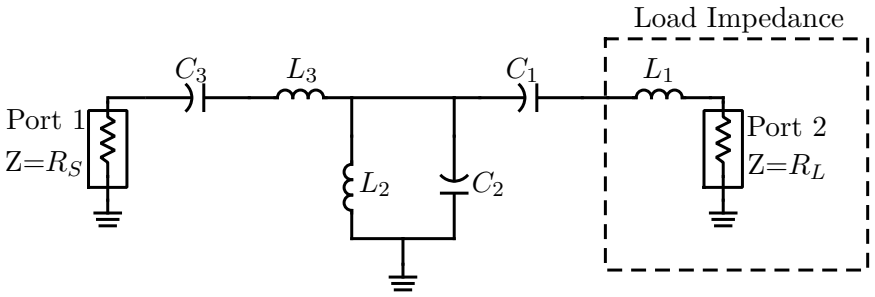


Figure 4.3: Bandpass matching network with lumped components

for the lumped elements of the matching networks is in Table 4.1.

Elements	L_1	C_1	L_2	C_2	L_3	C_3	R_S	R_L
Matching Network1	10 nH	7 pF	35 nH	2 pF	12 nH	6 pF	99 Ω	100 Ω
Matching Network2	20 nH	3.5 pF	25 nH	2.7 pF	16 nH	4.3 pF	105 Ω	100 Ω

Table 4.1: Element values of matching networks used in matching performance comparison

Using Agilent Design Software (ADS), the response of the reflection coefficients of the two matching networks are shown in Figure 4.4.

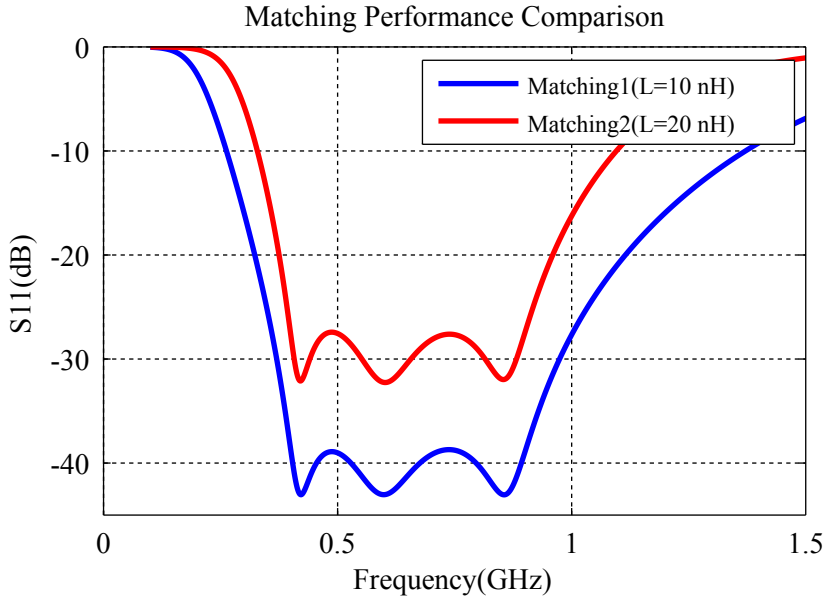


Figure 4.4: Comparison of matching network Performance for two different loads

As shown in Figure 4.4, the blue line indicates the reflection from port 1 of the first matching network which achieved a S_{11} close to -38 dB across the operation frequency. In comparison with the red line that shows the reflection coefficient of the second matching network which achieved a S_{11} of -27 dB across the operation bandwidth. This result indicates that the increase in quality factor of the load decreases the performance of the matching network across a fixed bandwidth.

The only why to further improve the performance of matching network 2, is to increase the order of the network. Increasing the order does not completely solve the problem, since there is also an upper limit reached, when the increased performance does not outweigh the increase in cost and size of the network. Matthaei, Young and Jones [36] showed that increasing the order of the network beyond 4 does not justify the performance gained, due to the increased loss of the elements in the matching network.

4.3 Wide-Band Matching Technique for Real Impedances

When a match over a very wide-band is required filter techniques become more attractive because they allow a quick calculation for the starting values of the lumped elements in the matching network. The method that is considered is to derive the low pass prototype of the Chebyschev equal ripple transfer function for different real impedances for the source and load. First the characteristics of the Chebyschev function are explained, secondly the basic design equations for the calculation of the low pass prototype elements are given followed by an example detailing the matching procedure.

4.3.1 Characteristics of The Chebyshev Transfer Function

In general the amplitude squared transfer function of a filter network is written as [37]

$$|S_{21}|^2 = \frac{1}{1 + \epsilon^2 T_n^2(\omega)} \tag{4.4}$$

where ϵ is the ripple constant and $T_n(\omega)$ is some filter characteristic function. By selecting $T_n(\omega)$ as a Chebychev function of the first kind it will have the following form [37]

$$T_n(\omega) = \begin{cases} cos(ncos^{-1}(\omega)), |\omega| \geq 1 \\ cos(ncosh^{-1}(\omega)), |\omega| \leq 1 \end{cases} \tag{4.5}$$

where n is the order of the function and ω is the angular frequency in rad/s. The Chebychev function is selected for filter and matching networks as it gives a good approximation to the ideal response by selecting the passband ripple ϵ.

The insertion loss S_{21} for the Chebychev transfer function is plotted in Figure 4.5. The blue line indicates a Chebychev response of a first order Chebychev polynomial and the green and red lines correspond to higher order Chebychev polynomials.

An advantage of increasing the order of the Chebychev function is that there is a sharper roll-off improving the selectivity of the matching network. This is indicated by the red line of the third order Chebychev polynomial. As the cut-off frequency of $\omega = 1$ rad/s is reached, the roll-off becomes sharper compared the lower order polynomials.

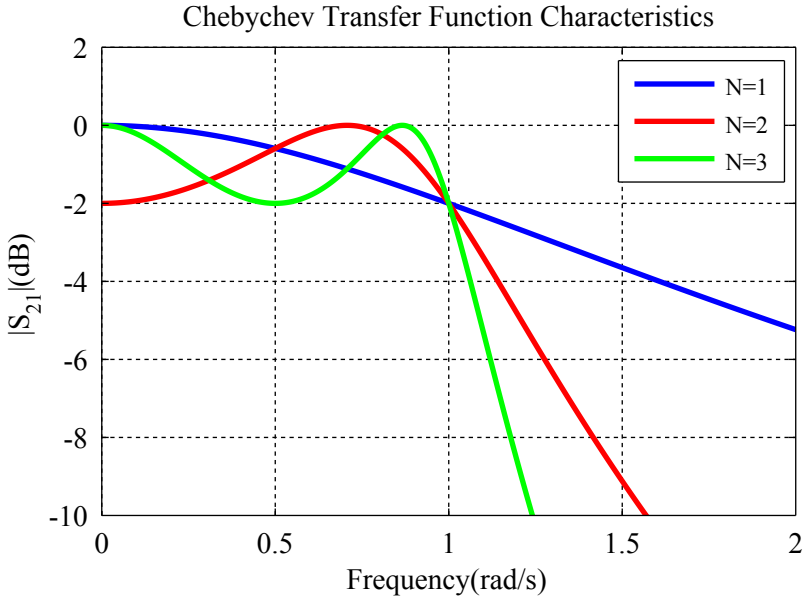


Figure 4.5: Chebychev transfer function characteristics

4.3.2 Design equations for Chebychev lowpass prototype

An example of a 4th order low pass prototype matching circuit is shown in Figure 4.6.

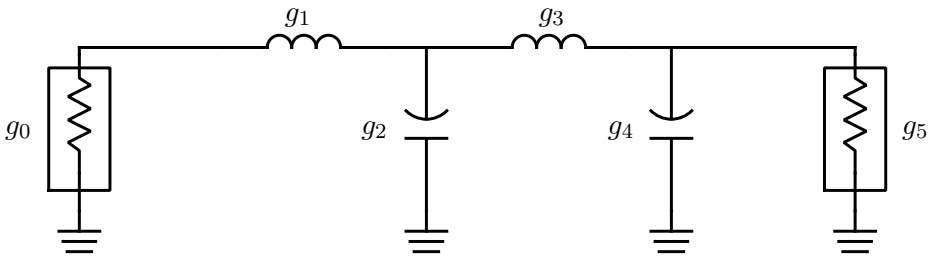


Figure 4.6: Low pass matching network

The element values (g-values) in Figure 4.6 have been normalised with frequency to produce a filter with a ripple bandwidth of 1 rad/s. For the case of $g_0 = 1$, the following design equations are used to calculate the g-values for the low pass prototype [37],

$$g_1 = \frac{2}{\gamma} sin\left(\frac{\pi}{2n}\right) \tag{4.6}$$

$$g_i = \frac{4sin\left[\frac{(2i-1)\pi}{2n}\right] sin\left[\frac{(2i-3)\pi}{2n}\right]}{g_{i-1}\left(\gamma^2 + sin^2\left[\frac{(i-1)\pi}{n}\right]\right)} \text{for}, i = 2, 3, ...n \tag{4.7}$$

$$g_{n+1} = \begin{cases} 1 & \text{for } n \text{ odd} \\ coth^2\left(\frac{\beta}{4}\right) & \text{for } n \text{ even} \end{cases} \tag{4.8}$$

where,

$$\beta = ln\left[coth\left(\frac{L_{Ar}}{17.37}\right)\right] \tag{4.9}$$

$$\gamma = sinh\left(\frac{\beta}{2n}\right) \tag{4.10}$$

There are two ways these equations are used to design matching or filter networks. The first is to specify L_{Ar} (dB) which is the size of the ripple in the passband. Equation (4.9) is used to calculate β and then the load impedance and low pass elements are calculated according to equations (4.6) to (4.8). This process is useful in filter applications where the load and source impedance are equal. The odd order Chebychev polynomial is then used to design filter networks.

The second method is to use the even order Chebychev function to design a matching network for a known source and load. Starting with equation (4.10) to calculate the parameter β, using the value of the known normalised load g_{n+1}. The next step is to calculate the low pass prototype values from the design equations (4.6) to (4.8) and scale the elements to the correct frequency and impedance level as follows [22]

$$L_k = \frac{Z_0 g_k}{\omega_c} \tag{4.11}$$

$$C_k = \frac{g_k}{Z_0 \omega_c} \tag{4.12}$$

where Z_0 is the characteristic impedance of the network, usually equal to 50 Ω and ω_c is the cut-off frequency in rad/s. The disadvantage of using this method is that the passband ripple is set for a given source and load. For the purpose of this thesis method two will be used in order to design matching sections for the LNA designed in chapter 5. This process will be explained next in an example.

4.3.3 Example impedance matching with real loads

For this example, the goal is to match a 100 Ω load to a 50 Ω source, using a fourth order Chebychev matching network as shown in Figure 4.6. The cut-off frequency required to be equal to 1 GHz.

Solution

- The first step in the design procedure is to normalise the load with respect to the source impedance.

- Next the parameter β is calculated from equation(4.8) and the design equations(4.6) to (4.10) are used to calculate the low pass prototype values.
- The third step is to scale the matching network elements to the correct frequency and impedance level with equation (4.11) and (4.12).

A matlab script was written in order to calculate the element values for the low pass matching network and the results are shown in Table 4.2

g-values:	g_0	g_1	g_2	g_3	g_4	g_5
	1	1.6818	1.1892	2.3784	0.8409	2
Scaled element values:	R_S	L_1	C_2	L_3	C_3	R_L
	50 Ω	13.3 nH	3.79 pF	18.9 nH	2.67 pF	100 Ω

Table 4.2: Calculated Low pass prototype values

The low pass matching network using the scaled element values are simulated in ADS and the response is shown in Figure 4.7. The red line indicates the magnitude of S_{21} which is the power delivered to the 100 Ω load. Clearly the Chebychev characteristic is indicated by the 0.5 dB ripple in the passband. As indicated by the blue line, a reflection coefficient equal to -10 dB is achieved across the bandwidth of operation. It is important to note that th fixed load R_L determines the ripple factor L_{ar} and the minimum reflection coefficient achievable for the matching network. This method provides a quick and easy approach to design a matching network with lumped elements for real loads and is used later in the design of single stage low noise amplifiers in chapter 5.

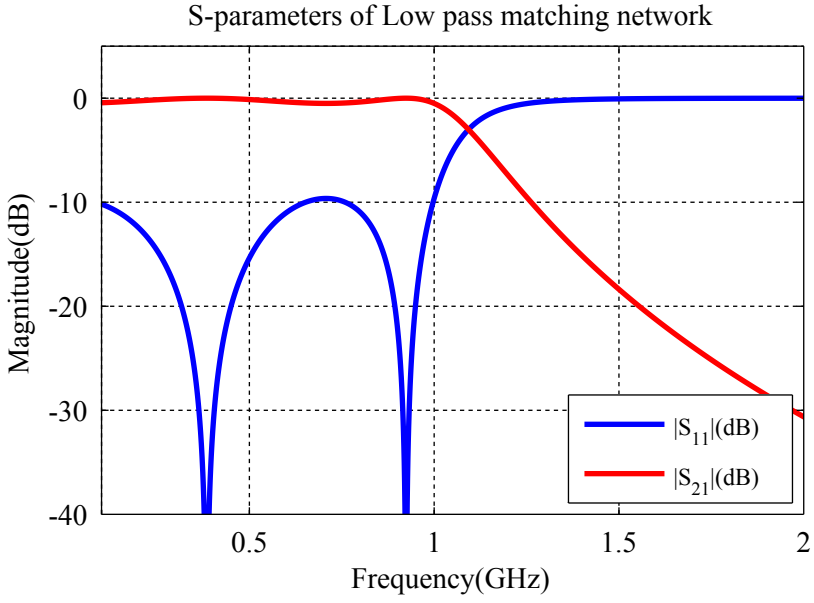


Figure 4.7: Low pass matching network response

4.4 A Wide Band Matching Technique for Complex Impedances

Fano [34], investigated the limitations of a matching network connected to a R-L or R-C load and derived a set of equations that are used to design a wide-band matching network for those types of loads. Fano's method relies on accurately modelling a component for example the input impedance of an amplifier as an R-L or R-C load. Then using the design equations, absorb the reactive part of the load into the matching network. In order to define the load correctly the following parameters have to be introduced, the load decrement and the reactance and susceptance slope. These parameters defines the load completely and is very useful later on in the design of a complex matching network.

4.4.1 Load Characterization

Assuming that the load has a perfect capacitive or inductive property. The first step in designing a complex matching network is to use this property by creating a resonator that resonates at the centre frequency ω_0. Depending on the reactive property of the load it is brought to resonance either by combining a capacitor and inductor in series or in parallel as shown in Figure 4.8(a) and (b).

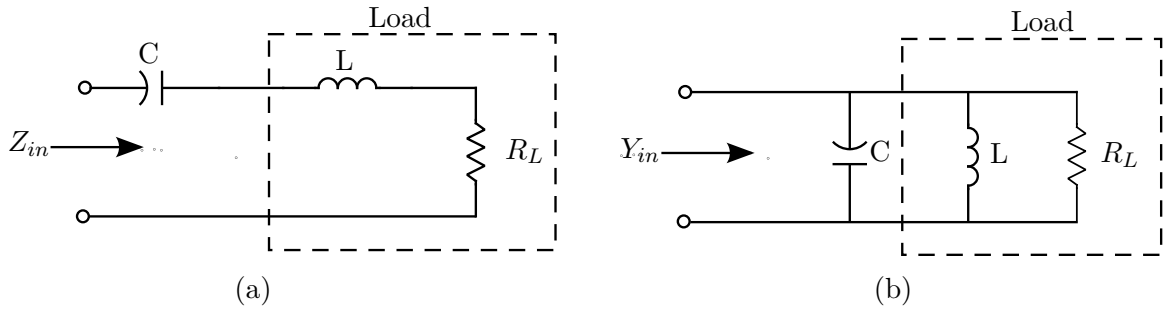


Figure 4.8: Load characterization (a) Series resonator (b) Parallel resonator

Calculating the values for either the capacitor or inductor for the series or shunt configuration shown in Figure 4.8 are done as follows [22]

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.13}$$

(4.14)

where ω_0 is the centre frequency of the operation bandwidth determined by taking the geometric mean of the two band edges ω_1 and ω_2 as follows [22]

$$\omega_0 = \sqrt{\omega_1 \omega_2} \tag{4.15}$$

In order to fully characterize the load. The input impedance of the ideal series RLC load or shunt configuration is determined and the theoretical response is shown in Figure 4.9. The blue line indicates an ideal resistor and the red line the reactive part of the load. The load decrement is defined as the inverse of the Q of the load, resonated at ω_0. In mathematical terms for a series

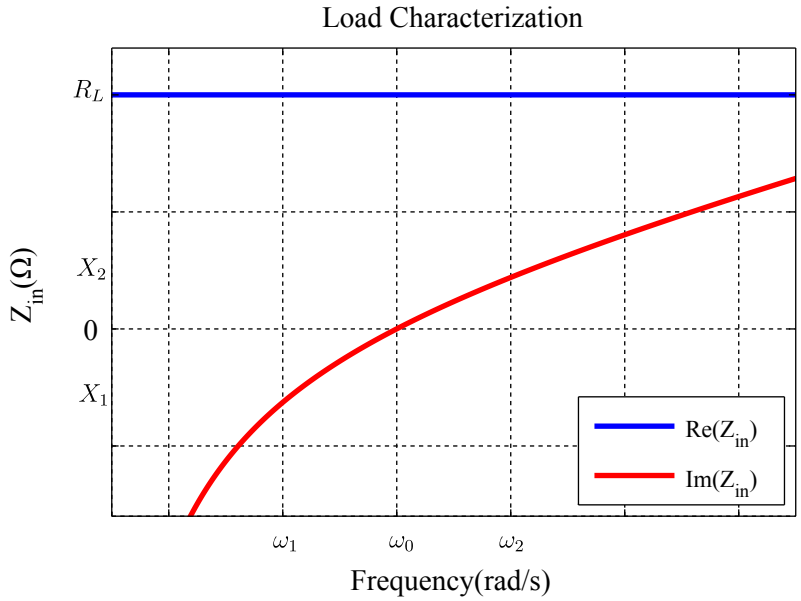


Figure 4.9: Input impedance of a series resonator

or parallel resonated circuit as shown in Figure 4.8(a) and (b) the load decrement is written as [36]

$$\delta = \frac{R_L}{X_L|_{\omega_1,\omega_2}} = \frac{G_L}{B_L|_{\omega_1,\omega_2}} \tag{4.16}$$

where R_L and G_L are the real part of the load and X_L and B_L are the imaginary part of the load measured at one of the band edges, ω_1 or ω_2. This is a convenient representation of the load resonated at the centre frequency, that is used in the calculation of the low pass prototype values for a complex load.

A different way of looking at the reactive part of the RLC load is to determine the reactance or susceptance slope for a series and shunt configuration as follows [37]

$$x = \frac{\omega_0}{2}\left.\frac{dX}{d\omega}\right|_{\omega_0} = \omega_0 L \tag{4.17}$$

$$b = \frac{\omega_0}{2}\left.\frac{dB}{d\omega}\right|_{\omega_0} = \omega_0 C \tag{4.18}$$

where equation (4.17) shows that the slope of the reactance part of the series resonator is dependant on the inductor L. This indicates that as the reactance slope x is increased the Q of the load also increases resulting in a decrease in the performance of the matching network. A higher quality factor as shown in section 4.2 decreases the values of the elements in the matching network, making it more difficult to realise the matching network for a given load.

4.4.2 Design equations for low pass prototype with a complex load

In general the low pass matching network with a complex load has the configuration shown in Figure 4.10. All the elements in the low pass matching network are normalised with frequency to 1 rad/s and with impedance using the real part of the load R_L.

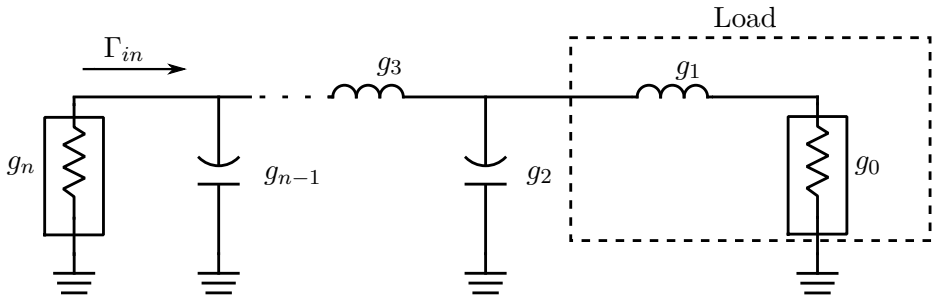


Figure 4.10: Low pass prototype with complex load

The ideal wide-band matching problem starts with assuming that there is a constant reflection over a given bandwidth from ω_1 to ω_2 as shown in Figure 4.11. In theory this ideal flat block response is achieved by an infinite degree polynomial using an infinite amount of elements in the matching network [38].

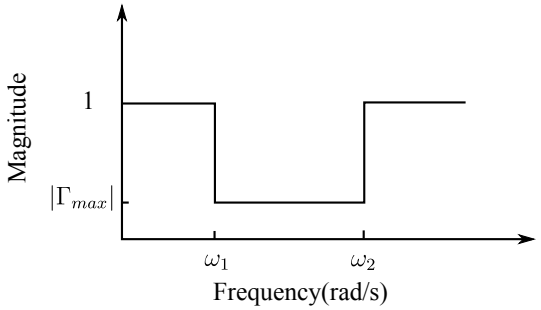


Figure 4.11: Ideal response of reflection coefficient for a given load

As shown by the integral equation (4.2) for a series R-L load the minimum reflection for this block response is written as [38]

$$(\omega_1 - \omega_2) ln\left(\frac{1}{|\Gamma_{max}|}\right) \leq \frac{\pi L_1}{R_L} \tag{4.19}$$

$$\Rightarrow min(|\Gamma_{max}|) = e^{-\delta\pi} \tag{4.20}$$

where equation (4.20) shows that the minimum reflection depends on the characteristics of the load as defined in equation (4.16) by the load decrement. The next step is to specify a function that approximates the ideal block response of the reflection coefficient using a finite amount of elements. A well known approximation is the Chebychev function $T_n(\omega)$ as specified in (4.5) and the reflection coefficient for a Chebychev matching network is defined as follows [38]

$$|\Gamma(\omega)|^2 = \frac{(K/\epsilon)^2 + T_n^2(\omega)}{(1+K^2)/\epsilon^2 + T_n^2(\omega)} \tag{4.21}$$

where K and ϵ are the loss and ripple factor of the transfer function. K is included because of the limitation set by equation (4.2) which indicates that a perfect match only occurs at discrete frequencies over a wide bandwidth. The calculation for the poles and zeros for the reflection coefficient of equation (4.21) are approximated by using the following sinusoidal relationships as

described in [38]

$$\frac{1+K^2}{\epsilon^2} = sinh^2(na) \tag{4.22}$$

$$\frac{K^2}{\epsilon^2} = sinh^2(nb) \tag{4.23}$$

$$\tag{4.24}$$

Substituting equation (4.22) and (4.23) into equation (4.21) gives expressions for the minimum and maximum reflection coefficient as follows [39]

$$|\rho|_{max} = \frac{cosh(nb)}{cosh(na)} \tag{4.25}$$

$$|\rho|_{min} = \frac{sinh(nb)}{sinh(na)} \tag{4.26}$$

where the goal is to minimize equation (4.25) under the constraint that the properties if the load are known and is written as

$$F = 2\delta = \frac{sinh(a) - sinh(b)}{sin(\frac{\pi}{2n})} \tag{4.27}$$

As indicated in equation (4.27) and (4.25) there are one degree of freedom remaining where one of the variables a or b can be chosen and a minimum for the maximum reflection coefficient can be determined. The method of Lagrange Multipliers is a method where a functions turning points can be determined subject to a constraint, defining the Lagrange multiplier as

$$b = \lambda a \tag{4.28}$$

Substituting equation (4.28) into (4.25) and then differentiating equation (4.25) with respect to the variable a as follows

$$\frac{d|\rho|_{max}}{da} = \frac{n\lambda(cosh(na)sinh(n\lambda a)) - acosh(n\lambda a)sinh(na)}{cosh^2(na)}$$

The turning points occur where $\frac{d|\rho|_{max}}{da} = 0$ and gives the following relationship

$$\lambda = \frac{tanh(n\lambda a))}{tanh(na)} = \frac{tanh(na)}{tanh(nb)} \tag{4.29}$$

Substituting equation(4.28) into (4.27) and differentiating with respect to a

$$\frac{dF}{da} = \frac{cosh(a) - sinh(\lambda a)\lambda}{sin(\frac{\pi}{2n})}$$

Setting $\frac{dF}{da} = 0$ gives the other relationship in terms of λ

$$\lambda = \frac{cosh(a)}{sinh(b)} \tag{4.30}$$

The final step is to set (4.29) equal to (4.30) and the result of the minimization condition is

$$\frac{tanh(na)}{cosh(a)} = \frac{tanh(nb)}{sinh(b)} \tag{4.31}$$

Equation (4.31) and (4.27) is solved simultaneously to determine the values of a and b. The solutions to this problem have been studied in great depth by Cuthbert [38] and a good starting point to obtain optimal solutions for the design parameters a and b is written as follows

$$a = sinh^{-1}(\delta(1.7\delta^{-0.6} + 1)sin(\frac{\pi}{2n})) \tag{4.32}$$

$$b = sinh^{-1}(\delta(1.7\delta^{-0.6} - 1)sin(\frac{\pi}{2n})) \tag{4.33}$$

where δ is the load decrement as calculated in (4.16) and n is the order of the matching network. Once these variables are known the following design equations are used to determine the low pass prototype values of the matching network shown in Figure 4.10

$$g_1 = \frac{2sin(\frac{\pi}{2n})}{x - y} \tag{4.34}$$

$$g_r g_{r+1} = \frac{4sin(\frac{2r-1}{2n}\pi)sin(\frac{2r+1}{2n}\pi)}{x^2 + y^2 + sin^2(\frac{r\pi}{n}) - 2xycos(\frac{r\pi}{n})}, \text{ for } r\text{=1,2...(n-1)} \tag{4.35}$$

$$\frac{g_n}{S} = \frac{2sin(\frac{\pi}{2n})}{x + y} \tag{4.36}$$

$$x = sinh(a) \tag{4.37}$$

$$y = sinh(b) \tag{4.38}$$

where g_1 is already known because it is part of the reactive part of the load and x and y are defined in (4.37) and (4.38). The parameter S has units of either conductance or resistance. S has the units of resistance if n is even and the units of conductance if n is odd.

After the low pass prototype values are calculated the circuit is scaled to the correct frequency and impedance level. For a bandpass network the following formulas are used to scale the low pass elements to bandpass resonators. For a series inductor the following transformations apply [22]

$$L_r = \frac{g_r}{\Delta\omega_0} \cdot R_0 \tag{4.39}$$

$$C_r = \frac{\Delta}{\omega_0 g_r} \cdot \frac{1}{R_0} \tag{4.40}$$

where $\Delta = \frac{\omega_2 - \omega_1}{\omega_0}$ to obtain the correct frequency scaling for each element. If a shunt capacitor is transformed from low pass to bandpass the following equations can be used

$$L_r = \frac{\Delta}{\omega_0 g_r} \cdot R_0 \tag{4.41}$$

$$C_r = \frac{g_r}{\Delta\omega_0} \cdot \frac{1}{R_0} \tag{4.42}$$

As indicated in the low pass to bandpass transformation, the parameter R_0 is the normalization impedance.

Design example of a matching network with a complex load

In this example the load, $Z_L = 100\ \Omega + 37.7\ \Omega$ and a third order $n = 3$ bandpass network is required from 400 to 900 MHz. The final matching network configuration is shown in Figure 4.12

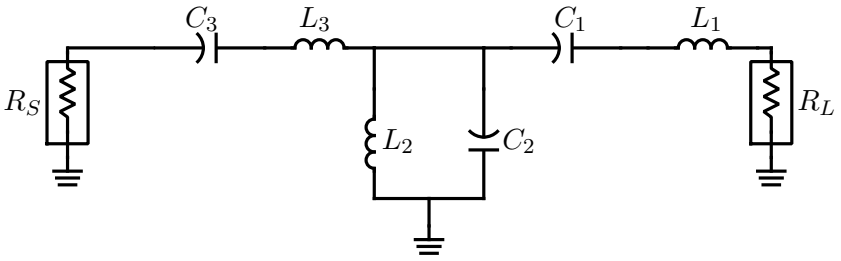
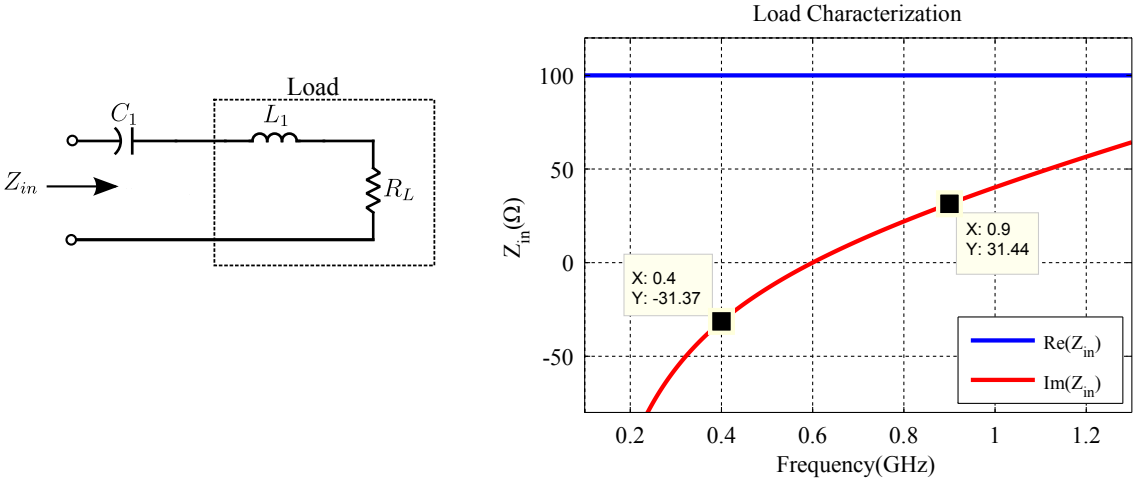


Figure 4.12: Bandpass matching network for complex load

Solution

The first step in the design procedure is to characterize the load over the band of operation as shown in Figure 4.13



(a) (b)

Figure 4.13: Noise Impedance Model (a) Equivalent circuit (b)Simulation Results

As shown in Figure 4.13 the load is resonated at the centre frequency $f_0 = 600$ MHz and the capacitance C_1 needed to cause the resonance is equal to 7 pF. The load decrement can be calculated from equation (4.16) as follows

$$\delta = \frac{R_L}{Im(Z_L)|_{f_1,f_2}} = \frac{100}{\sqrt{40.9 \cdot 27.2}} = 2.998$$

The parameters a and b can be found using equation (4.32) and (4.33), the results are as

$$a = sinh^{-1}(\delta(1.7\delta^{-0.6} + 1)sin(\frac{\pi}{2n})) = 1.8$$
$$b = sinh^{-1}(\delta(1.7\delta^{-0.6} - 1)sin(\frac{\pi}{2n})) = -0.24$$

Using equations (4.34) to (4.36) to calculate the low pass prototype values showed in Table 4.3

Final transformations to the bandpass network shown in Figure 4.12 are calculated by equations (4.39) to (4.42) and the results are shown in Table 4.4

g-values:	g_0	g_1	g_2	g_3	g_4
	1	0.314	0.626	0.365	0.986

Table 4.3: Low pass prototype values

Scaled Element Values :							
L_1	C_1	L_2	C_2	L_3	C_3	R_S	R_L
10 nH	7 pF	35 nH	2 pF	12 nH	6 pF	99 Ω	100 Ω

Table 4.4: Scaled Element Values

The final step is to simulate the matching network in a circuit simulator such as ADS. The results of the simulation for the circuit shown in Figure 4.12 are shown in Figure 4.14. The blue line represents the reflection from port 1 which shows a Chebychev ripple indicated by the three nulls in the passband below -40 dB for a source impedance of 99Ω. Normally a 50 Ω source is used but the real impedance matching technique explained in section 4.3 is used to transform the 99 Ω to 50 Ω. The red line in Figure 4.14 indicates the power transferred to port 2 from port 1.

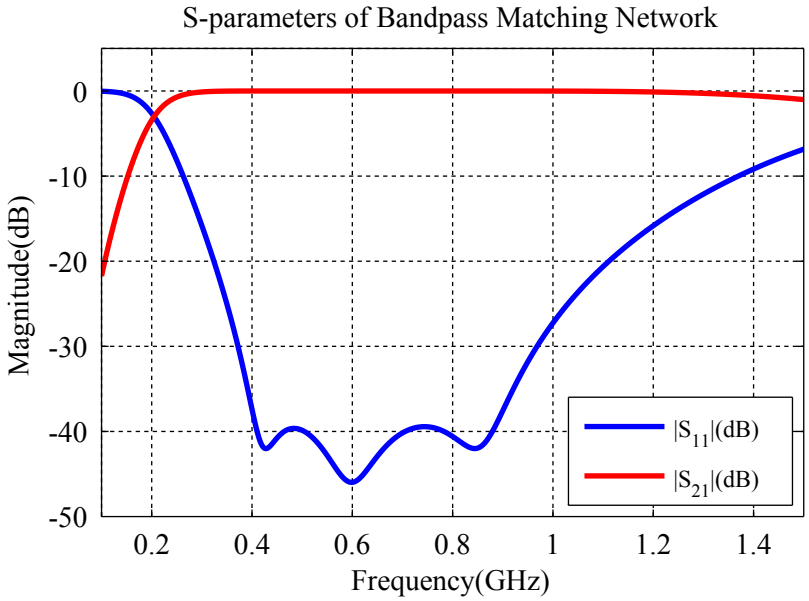


Figure 4.14: Bandpass matching network for complex load

Chapter 5

Low Noise Amplifier Design

The purpose of this chapter is to demonstrate the different factors in play when designing a wide-band LNA. Four designs are implemented, the first is a single stage frequency design at 500 MHz. This example shows the minimum achievable noise figure at a single frequency. The second and third designs are from 300–600 MHz and 300–900 MHz respectively, and both designs show the difficulties that arise when the bandwidth of a single stage amplifier is increased without the use of feedback.

Lastly a single stage amplifier is designed achieving both low noise and a flat gain profile from 350 MHz–1.2 GHz. In order to achieve this wide-band operation, sophisticated matching networks are needed, while negative feedback is used to achieve the flat gain response. All the designs are implemented using the same transistor from Infineon (HBT842ESD) [40] and the substrate from Rogers (4003C) [41] to ensure that the design techniques are comparable.

5.1 Single Frequency LNA Design (500 MHz)

5.1.1 Stability Analysis and Biasing

A Infineon HBT (BFP842ESD) transistor is chosen because of its low noise figure, high gain and low power consumption as discussed in section 3.4. From the data sheet(see appendix A) the transistor is biased at $V_{ce} = 2.5$ V for a collector current of $I_c = 5$ mA to achieve the lowest NF for optimum performance.

Before the biasing network is added the device is first stabilised using the vendor supplied S-parameter data from Infineon, measured at $V_{ce} = 2.5$ V and $I_c = 5$ mA. Thereafter, the same method as described in section 3.2.1, is used to determine the value of R_{stab} in Figure 5.1. The load stability circles are plotted and a value of $R_{stab} = 60\ \Omega$ is determined as the minimum value necessary for a stable device. The results of the stability analysis up to 10 GHz are shown in Figure 5.2.

The blue line in Figure 5.2 represents the load stability factor, whereas the black line is for the source stability factor. Both stability factors are greater than 1, which means that the device is unconditionally stable and any matching network can be added to the device for the frequency

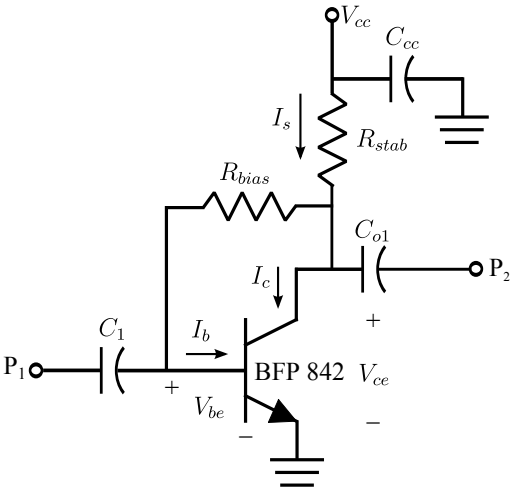


Figure 5.1: Amplifier with Stability and Biasing Resistors

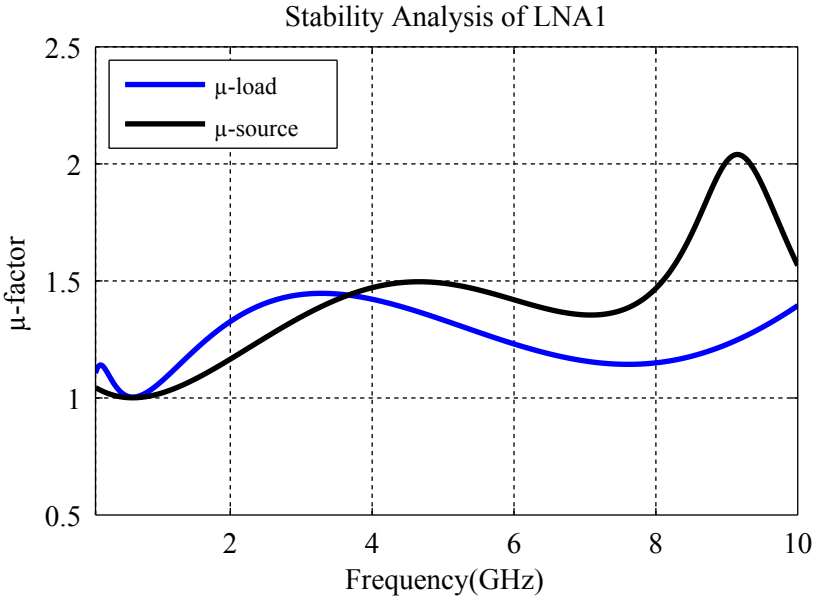


Figure 5.2: Amplifier Stability

of interest, giving the designer much more freedom in selecting matching elements. Caution should be taken at the lower frequencies where the stability factor approaches instability but is still greater than 1.

As shown in Figure 5.1, R_{stab} is incorporated into the biasing network to minimize the complexity of the structure and simplify the biasing network calculations. Since the value of R_{stab} is known, the only variables left to be determined for the biasing network are R_{bias} and the supply voltage

V_{cc}. The supply voltage is determined by taking a KVL loop as follows

$$-V_{cc}+I_c(1+\frac{1}{\beta})R_{stab}+V_{ce}=0 \tag{5.1}$$

$$\Rightarrow V_{cc}=I_c(1+\frac{1}{\beta})R_{stab}+V_{ce} \tag{5.2}$$

$$=5mA(1+1\frac{1}{260})(60)+2.5$$

$$=2.8\ V$$

where β is the DC current gain equal to 260 taken from the data sheet showed in appendix A. The value for the biasing resistor is determined from the other KVL loop as follows

$$V_{cc}+i_sR_{stab}+i_bR_{bias}+V_{be}=0 \tag{5.3}$$

$$\Rightarrow R_{bias}=\frac{V_{cc}-V_{be}+I_sR_{stab}}{I_b}=105\ k\Omega$$

The value for the RF decoupling capacitor C_{cc} is selected as 3300 pF to ensure good grounding for the RF path and to decouple the DC from RF. The DC block capacitors C_1 and C_{o1} are determined next when the matching networks are added to the amplifier.

5.1.2 Ideal amplifier response

Consider the circuit shown in Figure 5.3, where the input and output matching networks are added to the amplifier. The noise matching network, which consists of the shunt inductor L_2 and

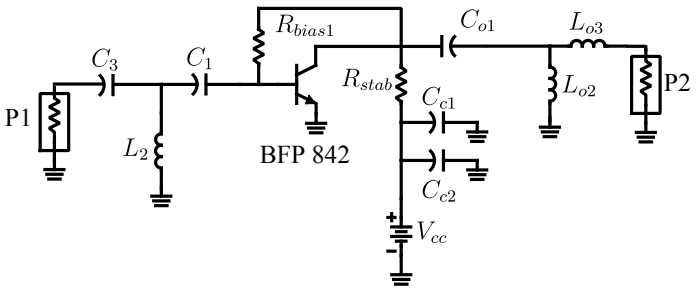
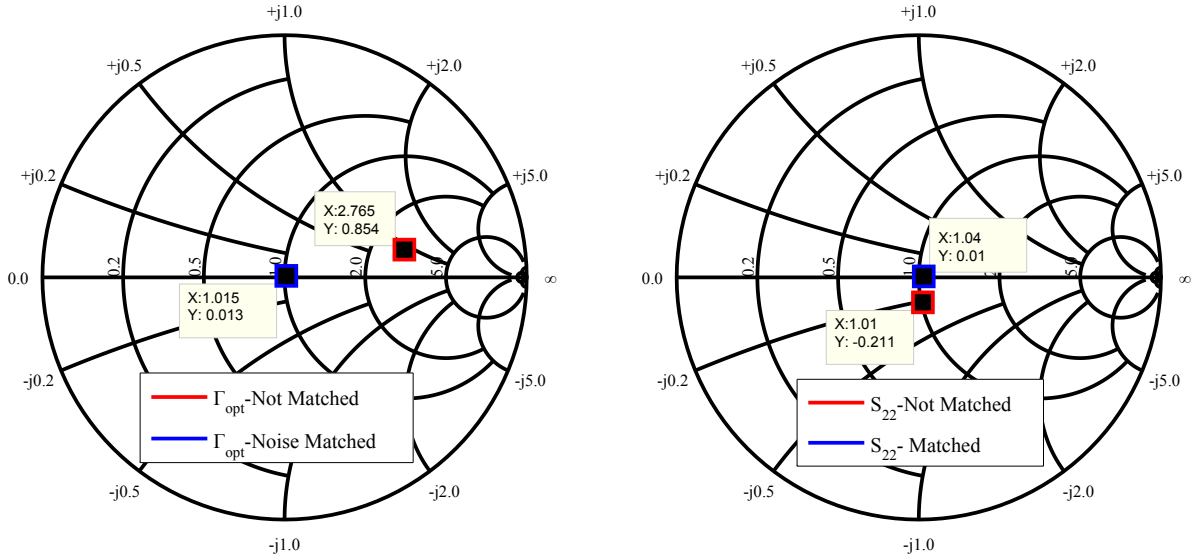


Figure 5.3: Circuit schematic of single frequency amplifier

series capacitors C_1 and C_3, is determined by simulating the optimum noise reflection coefficient Γ_{opt} shown in Figure 5.4(a). The red square indicates the optimum noise reflection coefficient before the matching network is attached. The capacitor C_1 is incorporated into the matching network and the value is determined as follows: if the capacitor value selected is too small the optimal gamma point is at the open circuit part of the smith chart. The value of the capacitor is increased so that the point on the smith chart does not get affected by the capacitor resembling a short circuit. A value of 47 pF is determined to be the optimum value for C_1.

The next step is to use the L-section technique described in [22] to determine the values for the parallel inductor L_2 and the series capacitor C_3. First L_2 is added in parallel and the value is changed until the $r=1$ circle on the smith chart is reached. There after C_3 can be added in



(a) (b)

Figure 5.4: Smith Chart of Input and Output Matching Networks (a) Noise (b) Maximum power transfer

series until the centre of the smith chart is reached as shown in Figure 5.4(a) by the blue line.

L_2 and C_3 are determined using the standard single frequency matching techniques described in [22]. The output impedance is determined using ADS and then the same matching procedure is followed as for the input matching network the determine the output matching network. The final results of the input and output matching network can be viewed in Table 5.1

Inductors:	L_2	L_{02}	L_{03}
	22 nH	112 nH	7.37 nH
Capacitors:	C_1	C_3	C_{o1}
	47 pF	4.3 pF	26.5 pF

Table 5.1: Calculated values for Matching Networks

The S-parameters of the complete single frequency amplifier with ideal components is shown in Figure 5.5(a) where the gain of the amplifier is indicated by the blue line. A high gain of 20 dB is achieved at the operating frequency, and the output reflection coefficient S_{22} is below -30 dB. The input reflection coefficient S_{11} is equal to -2.5 dB at the operating frequency as indicated by the black line. The input is matched for noise and in most LNA designs will result in a poor input power match because of the big difference in optimum impedance for noise and maximum power transfer. A minimum NF of 0.45 dB is achieved at 500 MHz as showed in Figure 5.5(b) by the blue line.

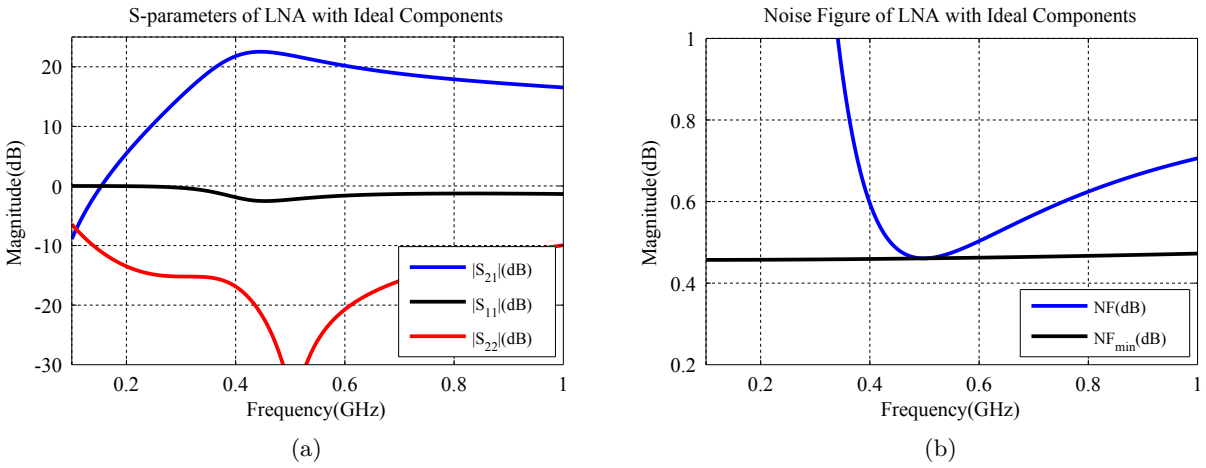


Figure 5.5: Simulation results of LNA with ideal components (a) S-Parameters (b) Noise Figure

5.1.3 EM-Simulation

The final step in the single frequency design process is to include all component losses and possible EM coupling in the layout. A Rogers 4003C, 0.508 mm substrate [41] is chosen for the design. The thin substrate will reduce the fringing effects caused by the micro strip tracks and minimise the coupling between components which could cause resonances and instability. The layout for the final design is showed in Figure 5.6, where the track widths are equal to 0.305 mm, which equals the size of the 0402 footprints used.

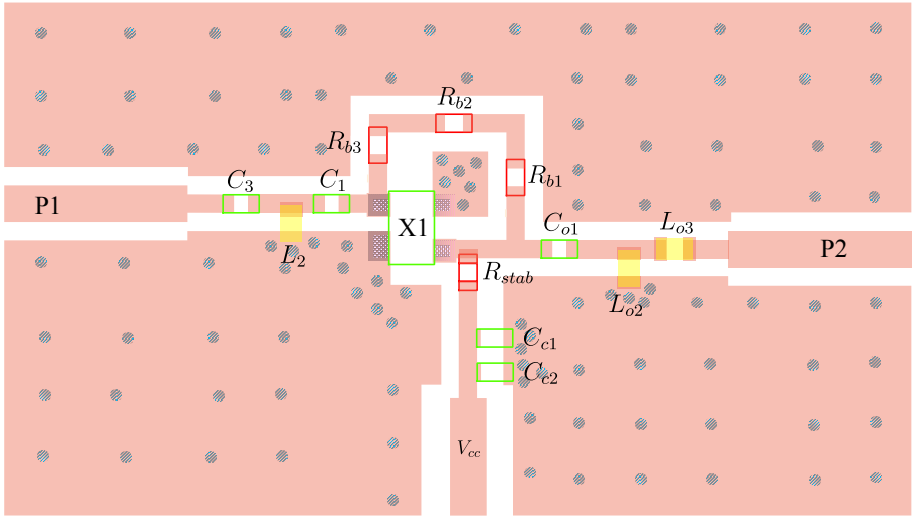


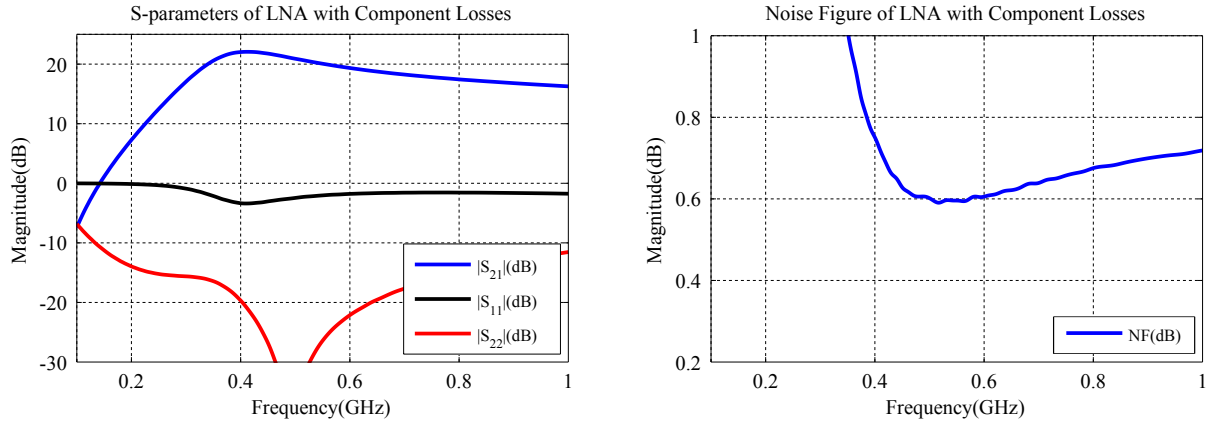
Figure 5.6: Layout of Single Frequency Amplifier

Using the full ADS analysis with layout and vendor supplied data, with a full spice model for the transistor, the capacitor C_3 had to be tuned in ADS by trial and error to 5 pF in order achieve the required results at 500 MHz. The output matching network also needed adjustment after the EM-simulation, L_{o2} is changed to 100 nH and L_{o3} to 5.1 nH. The inductors used are 0402HP models from Coilcraft and the capacitors are 0402 GCM models from Murata which

include component losses.

The final S-parameter results of the EM-simulation are shown in Figure 5.7(a) where the gain of the amplifier is above 20 dB at the design frequency as indicated by the blue line. The output reflection coefficient S_{22} is below 30 dB as showed by the red line.

In Figure 5.7(b) the noise figure of the LNA is shown by the blue line. It is important to note that the noise figure of the EM-simulation is 0.18 dB higher than in the ideal case, due to the losses the copper and the components contribute to the over all noise of the system. It is to be expected that when all the losses is included that the overall noise figure will be higher.



(a) (b)

Figure 5.7: EM-simulation results of LNA (a) S-Parameters (b) Noise Figure

5.2 Wide-Band LNA Design (300-600 MHz)

5.2.1 Stability Analysis and Biasing

In section 5.1, the BFP842 transistor is biased and stabilized up to 10 GHz, as shown in Figure 5.1 in section 5.1.1. The only variables that change are the DC block capacitors C_1 and C_{o1} that are dependant on the matching networks that are developed next.

5.2.2 Matching Network Design

The matching networks developed are based on the theory of wide-band matching in Chapter 4. The goal is to attach matching networks at each side of the amplifier as indicated in Figure 5.8. The input side is matched for minimum noise and the output for maximum power transfer.

5.2.2.1 Noise Impedance Estimation

The first step in the noise matching procedure is to estimate the optimal noise impedance. This is done by using Agilent Design Software (ADS) and plotting the optimal noise impedance vs frequency as shown in Figure 5.9(b) by the cyan and black lines. It is important to note that the

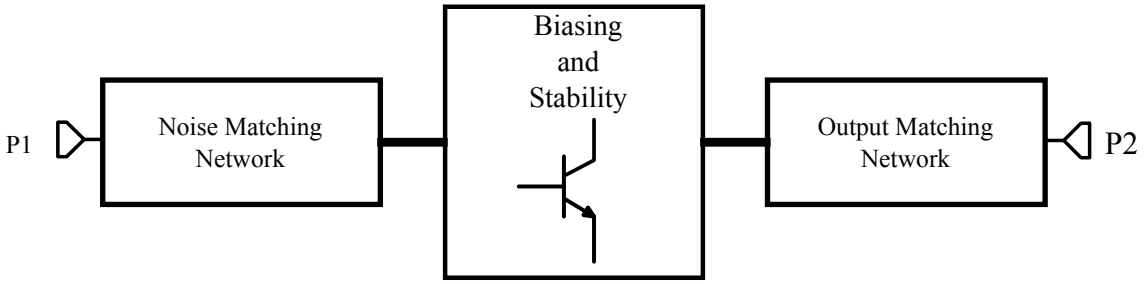
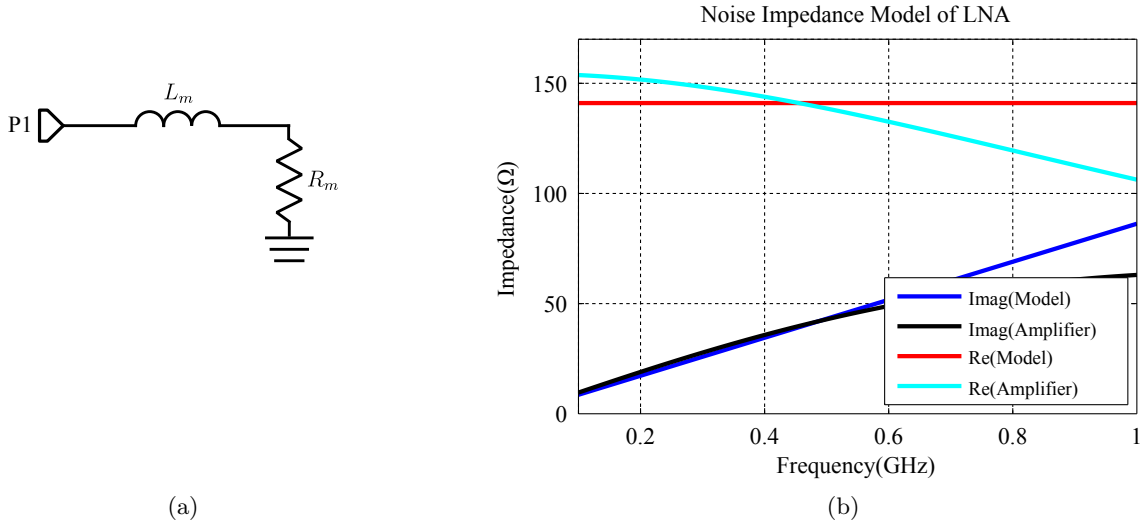


Figure 5.8: Amplifier with input and output matching networks

noise impedance changes with frequency and is modelled by an R-L or R-C circuit depending on the impedance of the transistor. An inductor $L_m = 13.7$ nH and resistor $R_m = 141\ \Omega$ is selected as the circuit best suited for the change in noise impedance, as shown in Figure 5.9(a). The red and blue lines in Figure 5.9(b) are the approximation model of the noise impedance.



(a) (b)

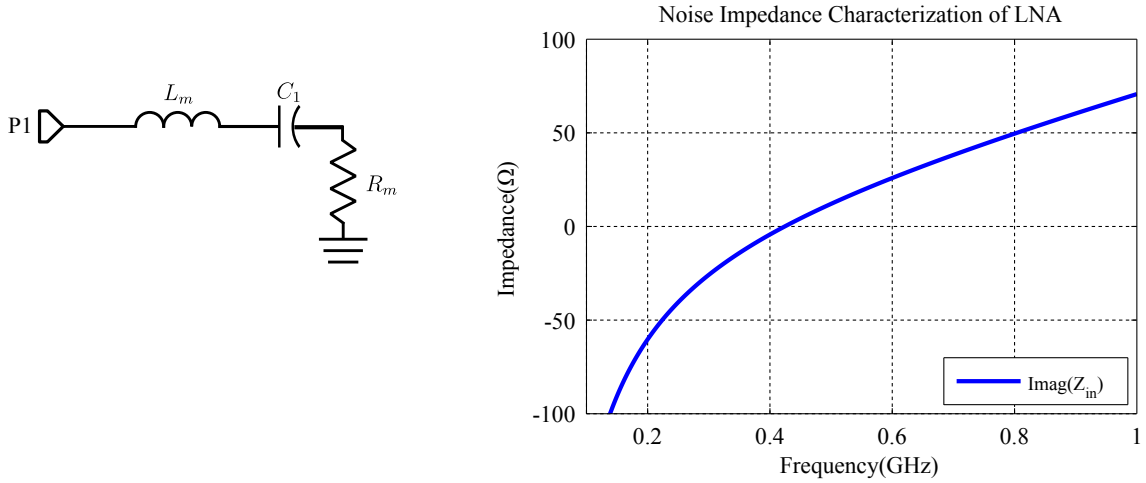
Figure 5.9: Noise Impedance Model: (a) Equivalent circuit (b)Simulation Results

5.2.2.2 Noise Matching Calculation

In order to characterize the optimum noise impedance $Z_{opt} = R_m + jX_m$, it is brought to resonance at $f_0 = 424$ MHz by adding a capacitor $C_1 = 10.6$ pF in series with the inductor L_m, as shown in Figure 5.10(a). The result of the imaginary part of the input impedance Z_{in} is shown in Figure 5.10(b). The load decrement is calculated from equation (4.16)

$$\delta = \frac{R_m}{Im(Z_{in})|_{f_1=600\text{ MHz}}} = \frac{141}{25.8} = 5.44 \tag{5.4}$$

where $Im(Z_{in})$ is determined by measuring the value at 600 MHz from Figure 5.10(b).
The elements of the noise matching network shown in Figure 5.11 are determined using δ and the complex load matching technique described in section 4.4, for the first three resonators C_1, L_1, C_2, L_2, C_3 and L_3. The remaining two resonators are calculated from the design equations used in section 4.3 for a real load transformation to 50 Ω and the results are shown in Table 5.2



(a) (b)

Figure 5.10: Noise impedance characterization: (a) Equivalent circuit (b) Simulation results

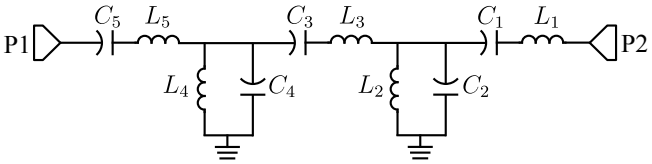


Figure 5.11: Noise Matching Network

Inductors:	L_1	L_2	L_3	L_4	L_5
	13.2 nH	91.1 nH	21 nH	19 nH	48 nH
Capacitors:	C_1	C_2	C_3	C_4	C_5
	10.6 pF	1.5 pF	6.7 pF	7.2 pF	2.8 pF

Table 5.2: Calculated values for Noise Matching Network

5.2.2.3 Output Impedance Estimation

The output matching network is determined using the same method as described in section 4.4. First the output impedance of the LNA needs to be estimated in order to determine the load decrement for the output matching network. The load estimation is shown in Figure 5.12(a) and (b) where the best suited circuit is a capacitor C_m in series with a resistor R_m. The red and blue lines in Figure 5.12(b) are the approximation of the output impedance of the amplifier with the input matching network attached to the input. Including the input matching network is important because the transistor is not a perfect unilateral transistor. This means that the input and output are not perfectly isolated and some modification is always needed after both matching networks are attached. The cyan and black lines in Figure 5.12 are the actual output impedance of the amplifier.

5.2.2.4 Output Matching Calculation

The second step in the output matching design is to use the estimated load to calculate the load decrement δ. Following the same procedure as described in section 4.4, where the output load

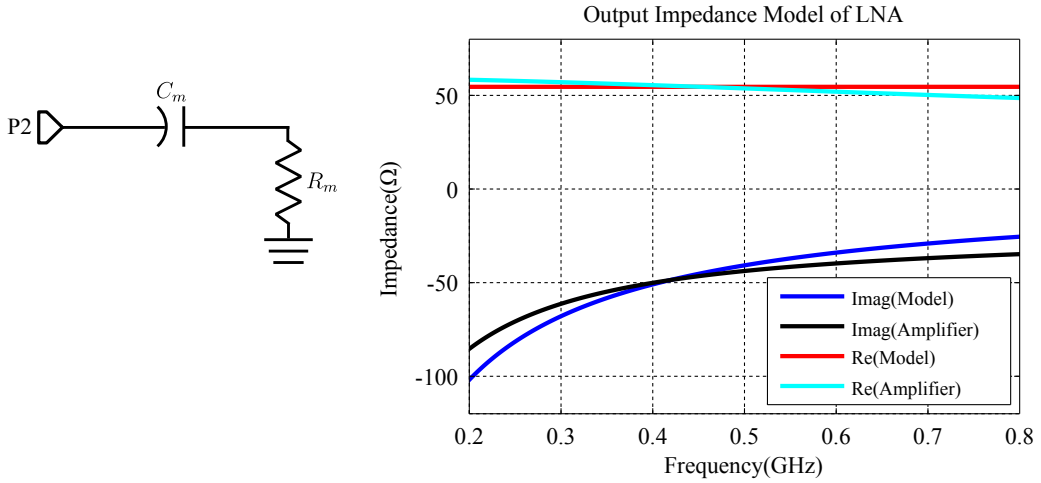


Figure 5.12: Output Impedance Model (a) Equivalent circuit (b) Simulation Results

is resonated at the centre frequency $f_0 = 424$ MHz and calculating the output load decrement from equation (4.16)

$$\delta = \frac{R_m}{Im(Z_{in})|_{f_1=600\text{ MHz}}} = \frac{55}{34} = 1.62 \tag{5.5}$$

The load decrement is used in the computation for the element values of the output matching network shown in Figure 5.13. The output matching network only consist of three resonators because the final impedance level after the calculation of the elements values using the complex matching technique described in section 4.4 is 50 Ω, therefore no extra real impedance transformation is necessary. The final results of the element values are shown in Table 5.3.

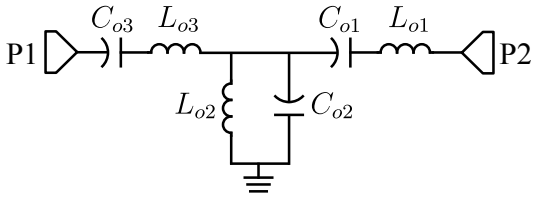


Figure 5.13: Amplifier with input and output matching

Inductors:	L_{o1}	L_{o2}	L_{o3}
	18 nH	17 nH	14.8 nH
Capacitors:	C_1	C_2	C_3
	7.8 pF	8.2 pF	9.48 pF

Table 5.3: Calculated values for output matching network

5.2.3 Ideal amplifier response

A complete circuit diagram of the amplifier with input and output matching networks are shown in Figure 5.14. The complete amplifier is simulated in ADS and the results of the S-parameters are shown in Figure 5.15(a). The black line indicates the gain is attenuated across the band of

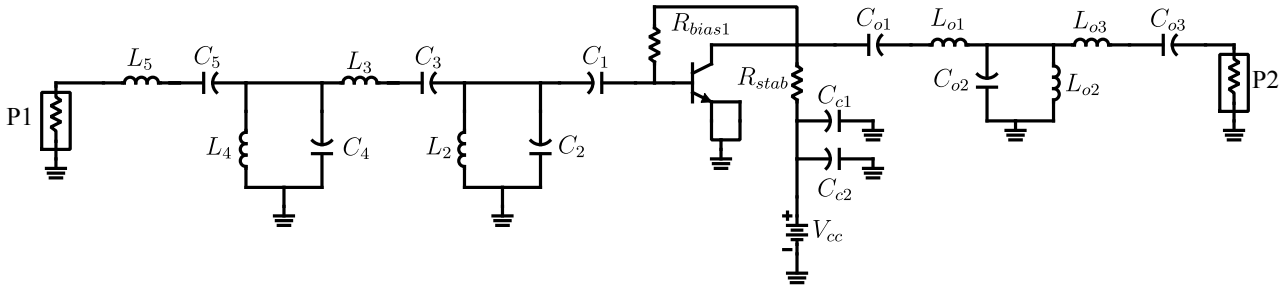


Figure 5.14: Amplifier with biasing, input and output matching networks

interest instead of having a flat response. As mentioned earlier after both matching networks are attached further optimization is needed to comprise for the loading effect the one matching network has on the other, since the transistor's input and output are not perfectly isolated from each other. This effect is also displayed in the output reflection coefficient which is below -20 dB as showed in Figure 5.14(a) and the noise figure indicated by the blue line in Figure 5.15(b) is not perfectly matched for minimum noise across the band of interest.

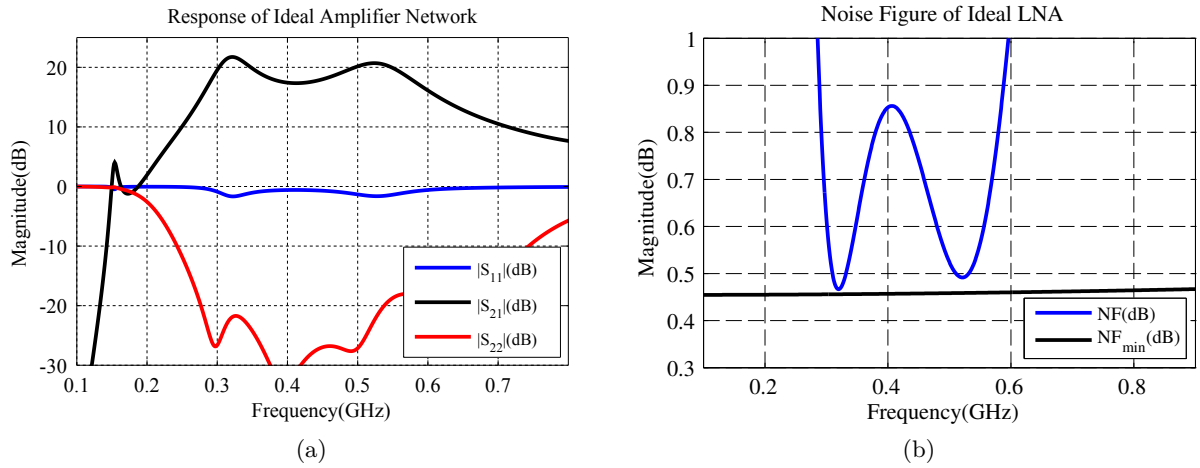


Figure 5.15: Simulation results of ideal LNA (a) S-Parameters (b) Noise Figure

5.2.4 Optimization and EM Simulation

The final step in the design procedure is to optimize the input and output matching networks to counter the loading affect the one network has on the other. In ADS the effect of the PCB tracks and box are taken into account with the EM-simulation environment. Figure 5.16 shows the layout for the low noise amplifier design.

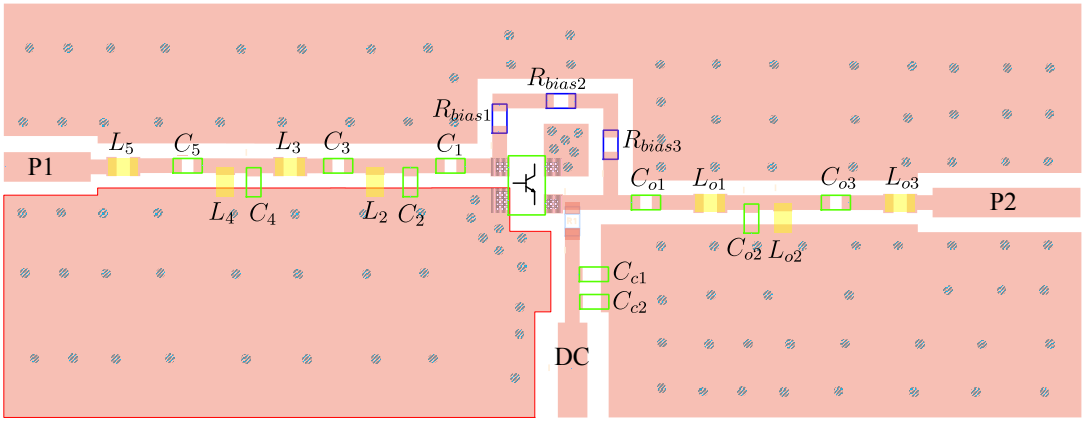


Figure 5.16: Layout of LNA

This layout is simulated in the EM-environment in ADS and then the ideal components are placed on top of the PCB and optimized to obtain the following element values for the amplifier shown in Table 5.4. The optimization procedure is explained in section 5.4

Inductors:	L_2	L_3	L_4	L_5	L_{o1}	L_{o3}	L_{o3}	
	197 nH	35 nH	13 nH	29 nH	19.6 nH	14.5 nH	15 nH	
Capacitors:	C_1	C_2	C_3	C_4	C_5	C_{o1}	C_{o2}	C_{o3}
	64 pF	2.8 pF	49 pF	12 pF	4.9 pF	10 pF	10 pF	9.4 pF

Table 5.4: Optimized values for the matching networks of the LNA

The S-parameter results of the optimized circuit are shown in Figure 5.17(a), where the black line indicates the gain of the amplifier which is above 20 dB and have an adequate flat response across the frequency range of interest. The red line is the output reflection coefficient S_{22} of the amplifier and is well below -20 dB. S_{11} indicates the input power match and is expected to be weak due to the fact that we matched for minimum noise and not for maximum power transfer for a 50 Ω system.

As shown in Figure 5.17(b), the noise figure of the amplifier is below 0.5 dB and is close to the minimum noise figure of the transistor. It is important to note that it is not possible to perfectly match the transistor for minimum noise across the entire frequency range because a perfect match can only occur at discrete frequency points as shown in section 4.2.

The final step in the design procedure is to attach vendor component models to the PCB which include losses for each component. A final response with the losses for all components included are shown in Figure 5.18(a) and (b), where the main difference is in the noise figure of the LNA which increased to 1 dB across a narrower bandwidth because of the component parasitics. The output power match indicated by the red line in Figure 5.18(a) decreased but is still below -20 dB. The gain of the amplifier is still above 20 dB and have a satisfactory flat response across the frequency range of interest.

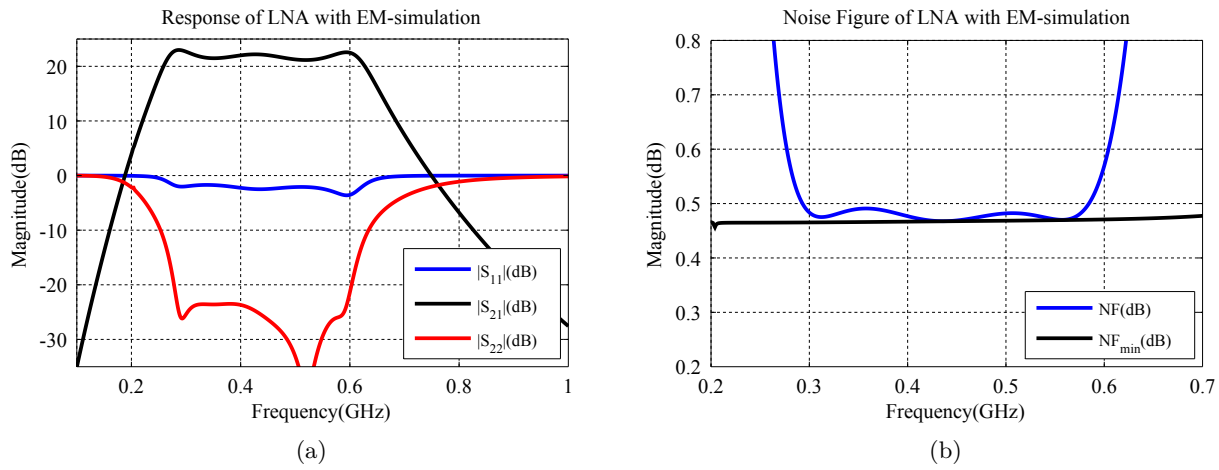


Figure 5.17: Simulation results of LNA after optimization and EM-simulation: (a) S-Parameters (b) Noise Figure

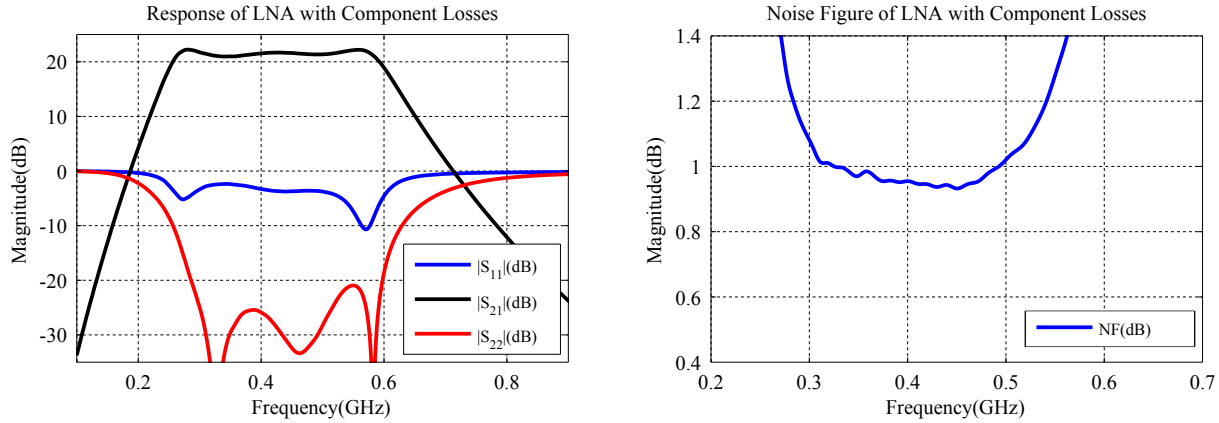


Figure 5.18: Simulation results of LNA with component losses (a) S-Parameters (b) Noise Figure

5.3 Wide-Band LNA Design (300-900 MHz)

5.3.1 Stability and Biasing

The same biasing as before is used where, the only variables that change are the DC block capacitors C_1 and C_{o1} that are dependant on the matching networks that are developed next.

5.3.2 Matching Network Design

The same procedure as, described in section 4.4, is followed to design the noise matching network. ADS simulation software is used to model the optimum noise impedance. The same approximate model consisting of a series inductor $L_m = 11.7$ nH and Resistor $R_m = 132\ \Omega$ as shown in Figure 5.9(a), is used.

The next step in the design procedure is to characterize the noise load by calculating the load decrement according to equation (4.16) at $f_0 = 519.6$ MHz

$$\delta = \frac{R_m}{X_m|_{f_1=900\text{ MHz}}} = \frac{131}{44} = 2.98$$

where R_m is the real part of the optimum noise impedance. The value of X_m is determined by the same method showed in section 4.4, where the load is resonated at the centre frequency f_0 = 519.6 MHz with a capacitor C_1 as shown in Figure 5.10(a). The imaginary part of the input impedance from this resonator is plotted and the value is taken at $f_2 = 900$ MHz .

The first resonator C_1,L_m where the inductor is part of the transistor model as shown in Figure 5.19 is determined by using the design equations (4.34) to (4.36). The remaining four resonators C_2, L_2 to C_5, L_6 are determined from the design equations (4.6) to (4.10) in order to calculate the g-values for the low pass prototype, and then use low pass to bandpass transformations 4.39 and 4.42 to obtain the final values shown in Table 5.5. A higher order real impedance matching network is needed to obtain the wider bandwidth from 300 - 900 MHz. The higher order matching network gives more freedom to the designer by increasing the order and adds more matching points across the band and achieves an improved noise match resulting in wider band performance.

Inductors:	L_2	L_3	L_4	L_5	
	21.5 nH	34.43 nH	15.68 nH	25 nH	
Capacitors:	C_1	C_2	C_3	C_4	C_5
	8 pF	4.4 pF	2.7 pF	6 pF	3.8 pF

Table 5.5: Calculated values for Noise Matching Network

After the noise matching network is attached to the amplifier, the output impedance is modelled as series capacitor C_m = 7.2 pF and resistor R_m = 52 Ω as shown in Figure 5.12(a). This model includes the DC block capacitor C_{o1} which is equal to 8 pF.

The output matching network, shown in Figure 5.19, is determined with the complex matching technique and the output load is characterized by resonating the load at the centre frequency f_0 by adding a series inductor L_{o1} to the load. Once the load decrement δ is calculated the rest of the element values can be determined using equations (4.34) to (4.36) to calculate the low pass prototype values. The low pass to bandpass conversions are then applied to scale the entire output matching network to the correct reference impedance of 50 Ω and frequency range. The final results for the output matching network are shown in Table 5.6

Inductors:	L_{o1}	L_{o2}	L_{o3}	L_{04}	L_{o5}
	13 nH	14 nH	22 nH	16 nH	8.8 nH
Capacitors:	C_{o1}	C_{o2}	C_{o3}	C_{o4}	C_{o5}
	7 pF	6.5 pF	4.1 pF	5.6 pF	10 pF

Table 5.6: Calculated values for Output Matching Network

5.3.3 Ideal amplifier response

The complete LNA is shown in Figure 5.19 and is simulated with ADS. The following results

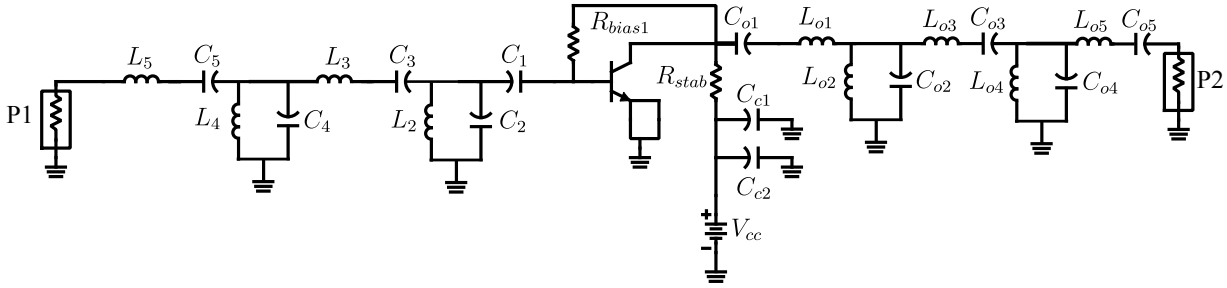


Figure 5.19: Amplifier with input and output matching

are obtained and shown in Figure 5.20. The gain of the amplifier as shown in Figure 5.20(a) is indicated by the blue line and it is important to note that there is a significant ripple across the band of interest and the gain of the amplifier drops from 22.3 dB to 18.7 dB across the entire bandwidth.

The noise figure also increases with frequency as indicated by the blue line in Figure 5.20(b). The ripple in the noise figure is caused by the fluctuating gain and improved results are achieved through optimization. As the loading effect of the output matching network on the input network is taken into consideration.

Note that this result indicates that the limit of the matching process is reached for this design. As the circuit model for the optimum source and load are very simple, the technique has an inherent bandwidth limitation. In this case, it is seen from the pronounced ripples in the response.

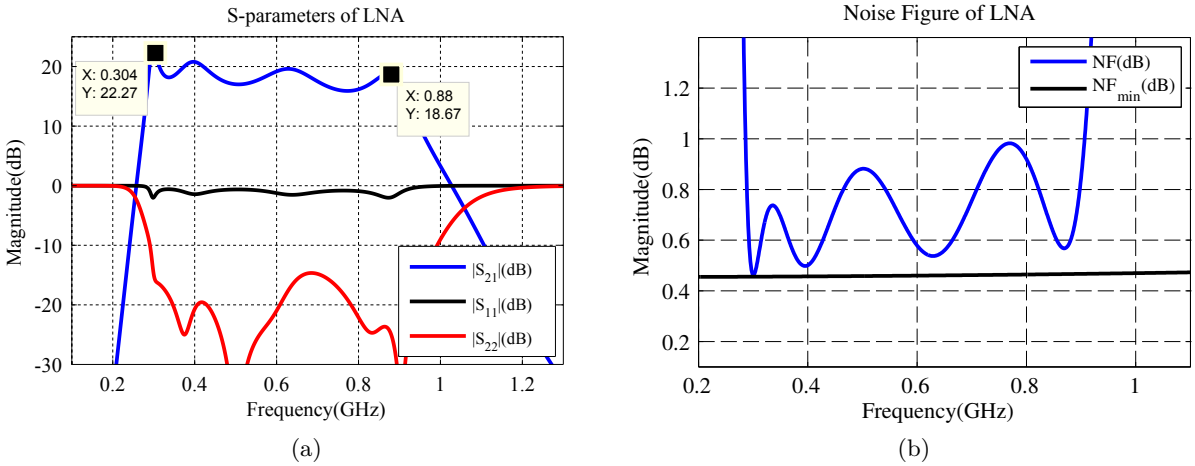


Figure 5.20: LNA results with Ideal components(a) S-parameters (b) Noise Figure

5.3.4 Layout and EM Simulation

In order to consider the effect that the PCB tracks and rf enclosure have on the amplifier. A PCB layout is created in ADS and shown in Figure 5.21. ADS design software enables the designer to simultaneously optimize the component values of the circuit as well as take the effects of the PCB into consideration. The substrate chosen is Rogers 4003C [41] with a height of 0.508 mm. The thin substrate reduces the fringing effects caused by the micro strip line which could lead to instability.

The optimization procedure(Newton search method) followed started with using the theoretical calculated element values in Table 5.5 and 5.6. The following goals are set in the optimization algorithm

$$NF_{error} = |NF - NF_{min}|$$
$$|S_{22}| < 20\text{dB}$$
$$|S_{21}| = 22\text{dB}$$

A quasi newton optimizer uses the Newton search method to calculate the new element values for the matching networks. It uses second order derivatives of the error function to find the quickest descending direction to minimize the goal. The noise figure of the LNA is optimized first using the co-simulation setup of ADS, where the circuit shown in Figure 5.19 is placed on top of the PCB layout in Figure 5.21. Thereafter, the output matching network is optimized by minimizing S_{22}.

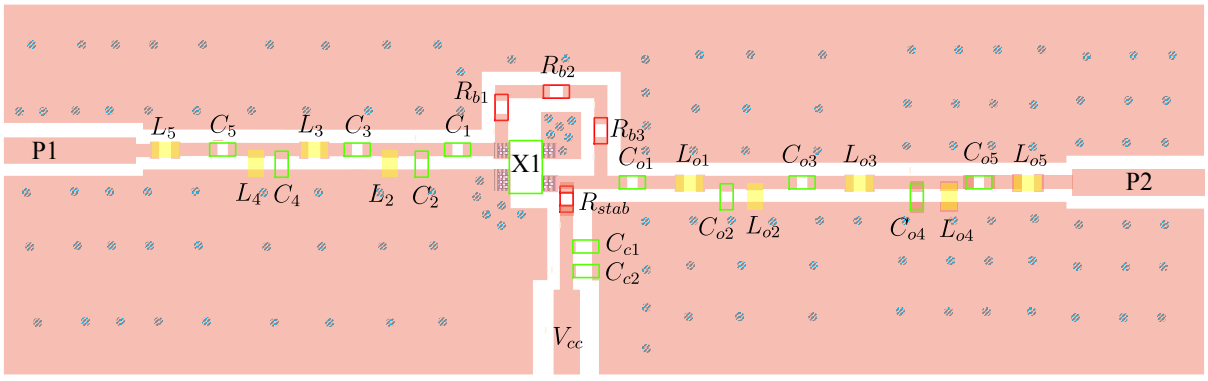


Figure 5.21: Amplifier with input and output matching

The final step in the co-simulation setup is to simultaneously optimize the input and output matching networks to be able take the loading effect that the one matching network has on the other into account. The final results of the elements for the matching networks is shown in Table 5.7

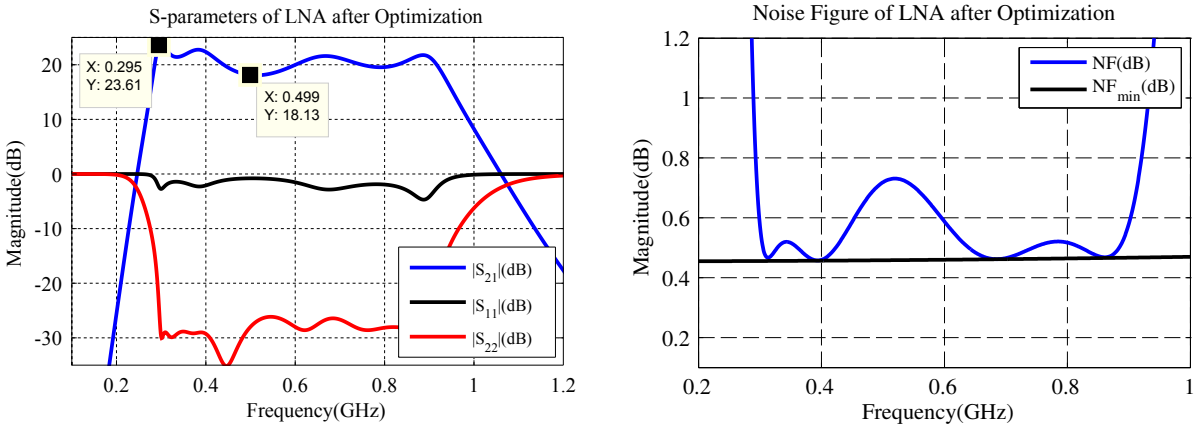
The S-parameters of the optimized element values of the amplifier are shown in Figure 5.22(a), where the blue line indicates the transducer gain of the amplifier and is above 18 dB across the entire bandwidth of 300-900 MHz. There is still a big ripple in the passband where the gain drops to 18.13 dB from 23 dB.

Inductors:	L_2	L_3	L_4	L_5	
	29.5 nH	41.8 nH	17.4 nH	23.6 nH	
	L_{o1}	L_{o2}	L_{o3}	L_{04}	L_{o5}
	12.5 nH	14.6 nH	18.8 nH	15.7 nH	6.6 nH
Capacitors:	C_1	C_2	C_3	C_4	C_5
	100 pF	2.4 pF	2.2 pF	5.5 pF	4 pF
	C_{o1}	C_{o2}	C_{o3}	C_{o4}	C_{o5}
	15 pF	7.2 pF	5 pF	5.9 pF	13 pF

Table 5.7: Optimized element values for Matching Networks

The output match of the amplifier is well below -20 dB indicated by the red line in Figure 5.22(a). The input reflection coefficient S_{11} is indicated by the black line and is very poor at -1.5 dB across the operation bandwidth. This is due to the fact that the input is matched for noise and a poor S_{11} is expected.

The NF of the device is below 0.8 dB across the operation bandwidth. As the bandwidth is increased it becomes difficult to match the amplifier perfectly across the entire bandwidth. A larger matching section can be used to improve the match but it also raises the over all noise level due to more components used in the matching network.



(a) (b)

Figure 5.22: LNA results with EM-simulation and Optimization(a) S-parameters (b) Noise Figure

The final step in the design procedure includes the component losses by using vendor supplied capacitor and inductor models from ADS. The inductors chosen are 0402 in size and the manufacturer is Coilcraft. Murata capacitors are chosen because they have a very small ESR value which should add minimum noise to the amplifier. The closest manufacturer component value where chosen and added to the PCB layout and the results from the EM-simulation with component losses are shown in Figure 5.23

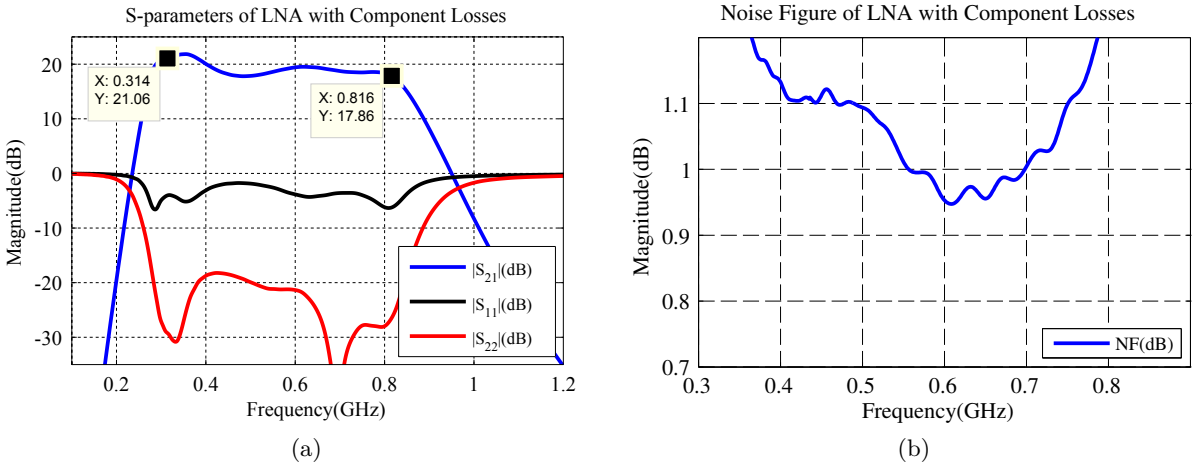


Figure 5.23: LNA results with EM-simulation and Component Losses (a) S-parameters (b) Noise Figure

As shown in Figure 5.23(a) the gain of the amplifier decreased slightly to 21 dB and the gain still drops to 17.86 dB at 800 MHz. The effect known as gain-roll off becomes quite a big factor as the bandwidth of the amplifier is increased beyond 2:1. The output reflection coefficient S_{22} is just above the 20 dB mark at 400 MHz. This shows that the component tolerances have quite a big impact and introduce some loss.

The noise figure of the LNA increases to 1.1 dB with component losses included as indicated by the blue line in Figure 5.23(b). The increase in noise figure is due to the fact that each component generates noise and the gain of the amplifier is not constant over the bandwidth causing a ripple in the noise figure as expected. A solution to obtain a flat gain response over a wider bandwidth is to either increase the number of matching elements or add feedback to the amplifier as shown in the following section.

5.4 Wide-Band LNA Design (350-1200 MHz) with Feedback

5.4.1 Stability, Feedback and Biasing

Consider the circuit, shown in Figure 5.24, where the first step in the design process is to stabilize the amplifier. The same stability procedure is used as described in section 3.2.3 where the output load stability circles are plotted using ADS. A minimum value for R_{stab} is determined to be equal to 60 Ω using the admittance circles of the Smith chart.

The feedback network consisting of a series resistor R_f and inductor L_f is added, and as discussed in section 3.3 when adding the feedback network it influences the stability, gain and noise figure of the device. The designer must be aware that the feedback network is very sensitive to parasitic effects of the components used. It is recommended to do a full wave EM-simulation of the layout with the feedback components before the matching networks are added. This minimizes the design time and the designer does not need to redesign the feedback network and adjust the matching networks if the device is properly stabilized. The starting values for the feedback

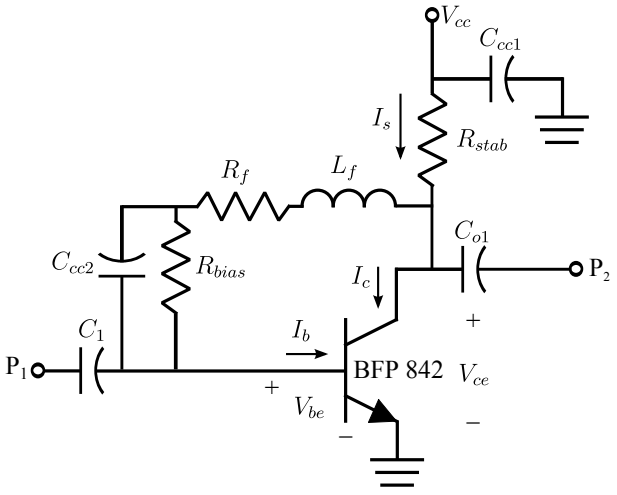


Figure 5.24: Amplifier with Feedback,Stability and Biasing

network are calculated using equation (3.22) and (3.23)

$$R_f = 50(1+10) = 550\ \Omega$$
$$L_f = \frac{550}{2\pi(1200MHz)} = 72.9\text{ nH}$$

The three variables R_{stab}, R_f and L_f have to be adjusted simultaneously by trial and error in order to obtain the correct response, which is a compromise between flat gain and low noise figure using the simulation software ADS. The design equations (3.22) and (3.23) assume that the input and output of the amplifier are matched for maximum power transfer to acquire the flat gain response. This causes the noise figure to increase and a good starting point for improving NF is to increase L_f and R_f in order to decrease the feedback and lower the noise figure. In return the improved noise figure alters the gain flatness but a compromise need to be made in order to achieve an optimal result. The final values for the stability and feedback network are shown in Table 5.8 and the simulation results of the amplifier with feedback are shown in Figure 5.25

Element Values:	R_{stab}	R_f	L_f
	100 Ω	2560 Ω	190 nH

Table 5.8: Optimized values for Stability and Feedback Network

As indicated by the blue line in Figure 5.25(a) the feedback decreased the gain at the lower frequencies and obtains an improved flat gain response which only decreased to 0.5 dB across the operation bandwidth. The black line shows the gain of the transistor data biased at $V_{ce} = 2.5$ V and $I_c = 5$ mA with no feedback. Excluding feedback the gain of the amplifier dropped to 2.8 dB from 300 MHz-1200 MHz. This shows that adding feedback improves the gain flatness.

The minimum noise figure after the feedback network is added, increased to 0.58 dB as indicated by the black line compared to the minimum noise figure of the transistor indicated by the red line in Figure 5.25(b). There is a trade off between flat gain response and noise figure that the

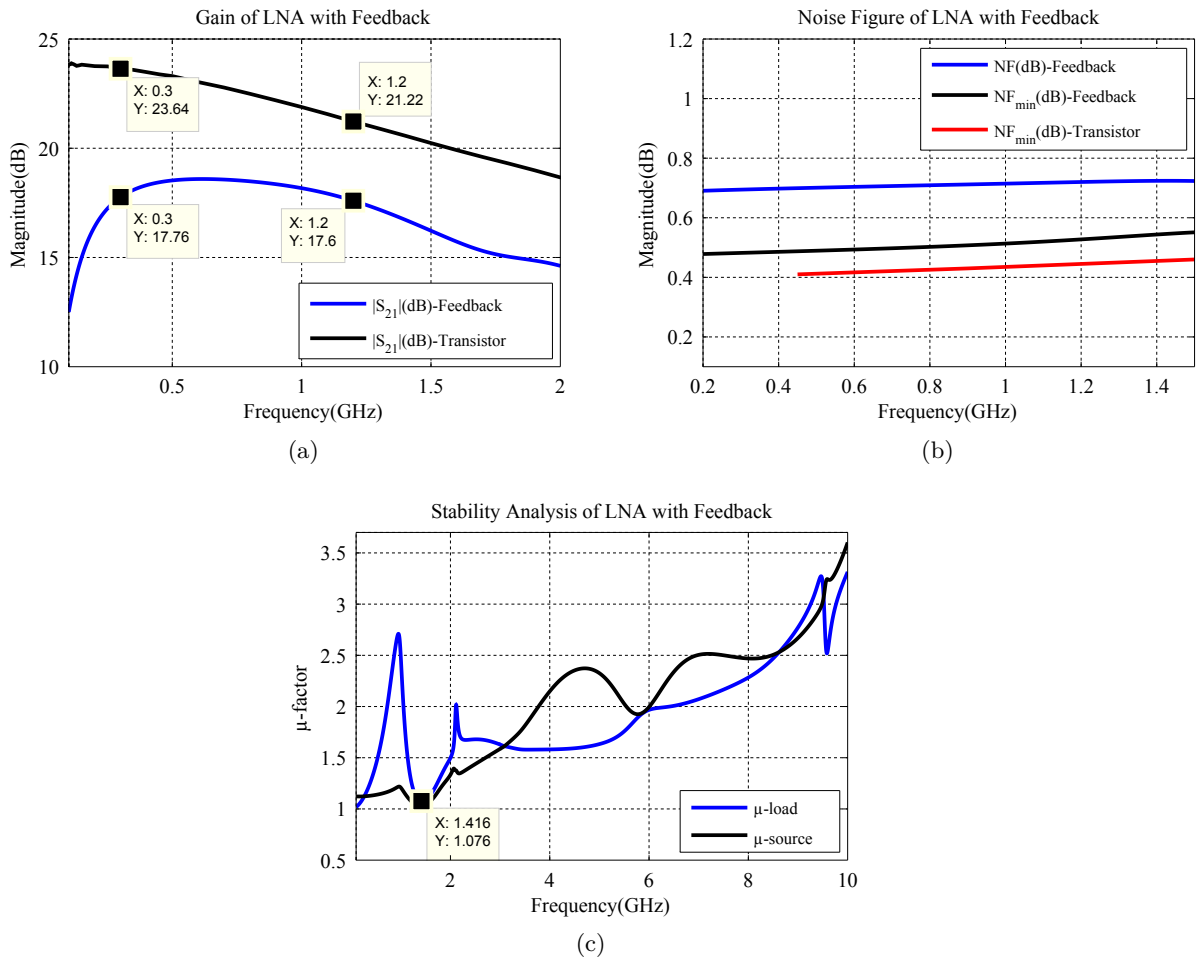


Figure 5.25: Simulation results with feedback and biasing (a) Gain (b) Noise Figure (c) Stability

designer needs to make in order to obtain an optimal result. One of the major drawbacks in feedback design is the complexity added to stabilize the device. As shown in Figure 5.25(c) the stability factor μ is plotted for the input and output of the device after the stability resistor R_{stab} is added. The $\mu-$load factor shows that the device approaches instability near 1.4 GHz, this is due to the Coilcraft 0402HP inductors which reaches its self resonating frequency at 1.4 GHz. If the device becomes unstable the gain will have to be decreased by adjusting the stability resistor.

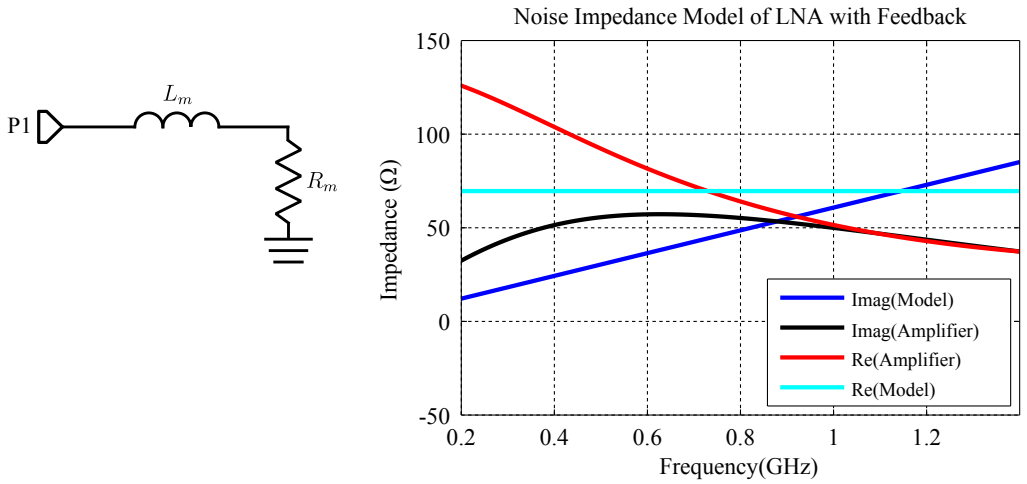
The biasing network is determined using the same method as described in section 5.1.1 by writing a voltage loop as shown by equation (5.1). The supply voltage is calculated to yield $V_{cc} = 3.4$ V and the biasing resistor is calculated by taking a voltage loop as indicated by equation (5.3) and the result for the biasing resistor is $R_{bais} = 88$ kΩ. The biasing resistor is decreased to include the R_f resistor in the DC biasing path.

A capacitor $C_{cc2} = 3300$pF is added in parallel with R_{bias} to split the RF and DC path. The choice of capacitor is up to the designer and the designer must ensure that it does not influence the band of operation or cause any unwanted resonances with the feedback inductor. C_{cc1} is also determined by simulation and a value of 0.027 μF is chosen to ensure that no external signals can influence the band of operation through the DC path. The other dc block capacitors C_1

and C_{o1} are determined in the matching section.

5.4.2 Matching Network Design

The first step in the matching procedure is to model the optimum noise impedance Z_{opt} of the device with the feedback network and component losses included. As shown in Figure 5.26(a)



(a) (b)

Figure 5.26: Noise Impedance Model (a) Equivalent circuit (b) Simulation Results

the optimum noise impedance is modelled as an inductor L_m in series with a resistor R_m. The results of the model is shown in Figure 5.26(b), where the blue line represent the imaginary part of the model for Z_{opt} and the black line represents the amplifier model with feedback. The real part of Z_{opt} is indicated by the red line in Figure 5.26(b) and the realistic model of the amplifier is shown by the cyan line. It is important to note that there is a big change in the real part of the noise impedance as the bandwidth increases. Optimization is needed after the matching network is added to compensate for the change in noise impedance level and any discrepancies between the approximation and realistic model.

The element values for the noise matching network as shown in Figure 5.27 are determined by combining the two matching methods described in chapter 4. The capacitor C_1 is determined by characterizing the load. It involves resonating the load at the centre frequency $f_0 = 648$ MHz and determining the load decrement δ from the input impedance of the resonator as shown in section 4.4. The next two resonators are determined by using the design equations (4.34) to (4.36) to calculate the low pass prototype values and then use the band pass transformations (4.39) and (4.42) to determine C_2, L_2, C_3 and L_3.

The next four resonators are determined by using the real impedance technique described in section 4.3. The four resonators transform a 77 Ω to 50 Ω using equations (4.6) to (4.10) to calculate the low pass values and then scale the low pass elements to the correct impedance and

frequency range using the bandpass transformations (4.39) and (4.42). The final values of the noise matching network are shown in Table 5.9

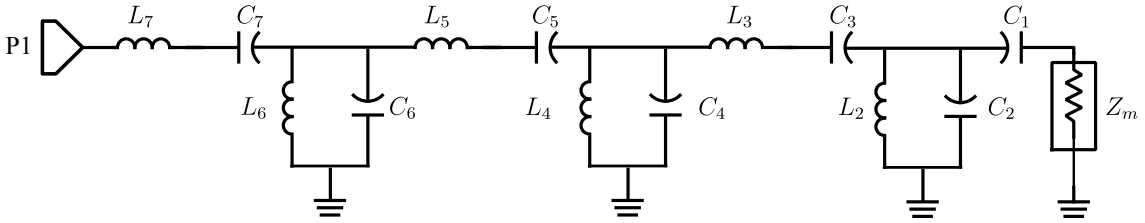


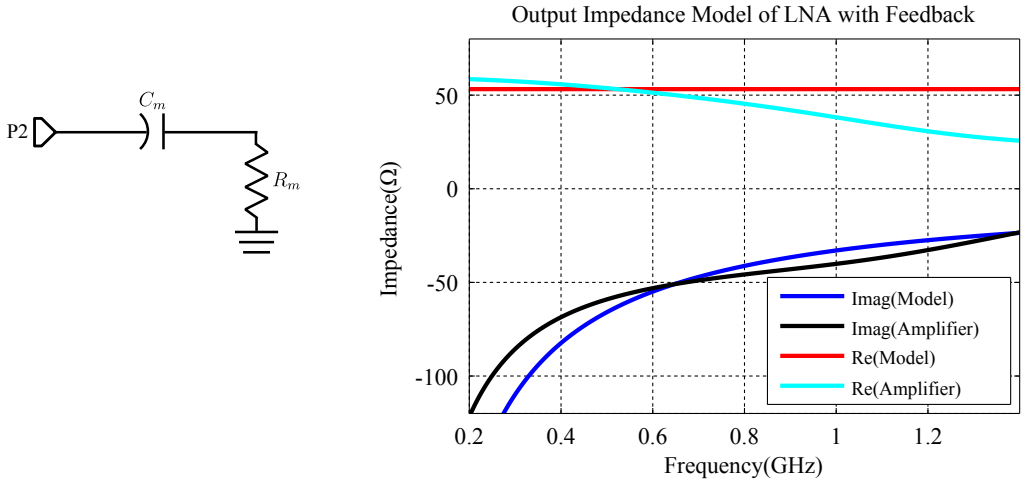
Figure 5.27: Noise Matching Network of LNA with Feedback

Inductors:	L_2	L_3	L_4	L_5	L_6	L_7	
	31 nH	7.4 nH	23.5 nH	17.5 nH	15.5 nH	12 nH	
Capacitors:	C_1	C_2	C_3	C_4	C_5	C_6	C_7
	7 pF	2.3 pF	9.5 pF	3 pF	4 pF	4.5 pF	6 pF

Table 5.9: Calculated values for Noise Matching Network

The output matching network is derived in the same way as the input matching network by using the wide-band impedance matching techniques developed in chapter 4. A different approach is taken for the output matching network, where the goal is to match the output of the amplifier for maximum power transfer.

Modelling the output impedance of the amplifier with a series capacitor C_m and resistor R_m as shown in Figure 5.28(a), which includes the capacitor $C_{o1} = 5$ pF. The results of the approximation model are shown in Figure 5.28(b) where the blue and red lines are the real and imaginary parts of the approximation model, and black and cyan lines are real and imaginary parts of the output impedance of the amplifier.



(a) (b)

Figure 5.28: Output Impedance Model (a) Equivalent circuit (b)Simulation Results

The first three resonators C_{o1}, L_{o1}, C_{o2}, L_{o2}, C_{o3} and L_{o4} of the output matching network shown in Figure5.29 are calculated by characterizing the output load and calculating the load decrement δ as shown in section 4.4. Once the load decrement is calculated the resonator values is determined using equations (4.34) to (4.36) as with the noise matching network. The final four resonators are determined using the real impedance technique, where equations (4.6) to (4.10) are used to calculate the low pass values and then scaled to form the bandpass network. The element values of the output matching network are shown in Table 5.10

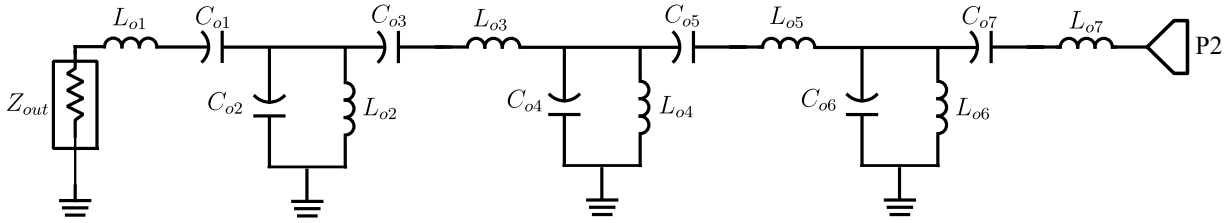


Figure 5.29: Output Matching Network of LNA with Feedback

Inductors:	L_{o1}	L_{o2}	L_{o3}	L_{04}	L_{o5}	L_{o6}	L_{o7}
	12 nH	19.5 nH	8.2 nH	19.5 nH	17 nH	12.3 nH	10.6 nH
Capacitors:	C_{o1}	C_{o2}	C_{o3}	C_{o4}	C_{o5}	C_{o6}	C_{o7}
	5 pF	3 pF	7.4 pF	3 pF	3.6 pF	4.8 pF	5.6 pF

Table 5.10: Calculated values for Output Matching Network

5.4.3 Layout and EM Simulation

A complete layout with input and output matching networks are shown in Figure 5.30. The following procedure are followed for the layout of the feedback network, where the value for the feedback resistor R_f and inductor L_f are split up into three resistors and inductors. The position for the resistors are very crucial since they are placed between each feedback inductor to minimize the chance of a resonator forming in the feedback loop, as shown in Figure 5.30.

Using a single component for the feedback inductor L_f causes problems since the self resonating frequency (SRF) of the inductor with a value of 220 nH moves into the band of operation. A solution to the problem is to divide L_f up into smaller values in series with each other, the lower valued inductors have a higher SRF and prevents the amplifier from oscillating.

After the layout is completed a full wave EM simulation is performed to include the parasitic effects introduced by the copper tracks and substrate. A Rogers 4003C substrate [41] with a thickness of 0.504 mm is chosen (see Figure 5.31) because the thin substrate reduces the fringing fields from the microstrip line. The substrate also has a very low loss tangent equal to 0.002 which reduces any losses in the circuit. The LNA is simulated in a closed RF enclosure with a box height of 10 mm as shown in Figure 5.31. Using a RF enclosure ensures that no external

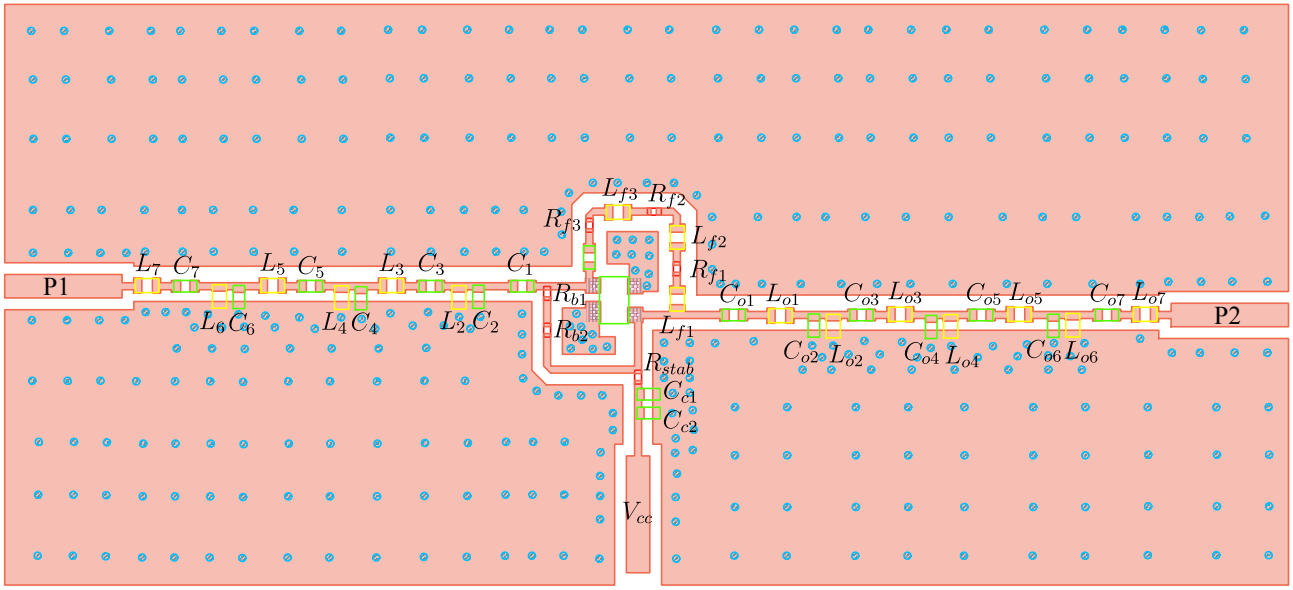


Figure 5.30: LNA Layout

signals, for example cellphone or television signals can interfere with the operation of the LNA.

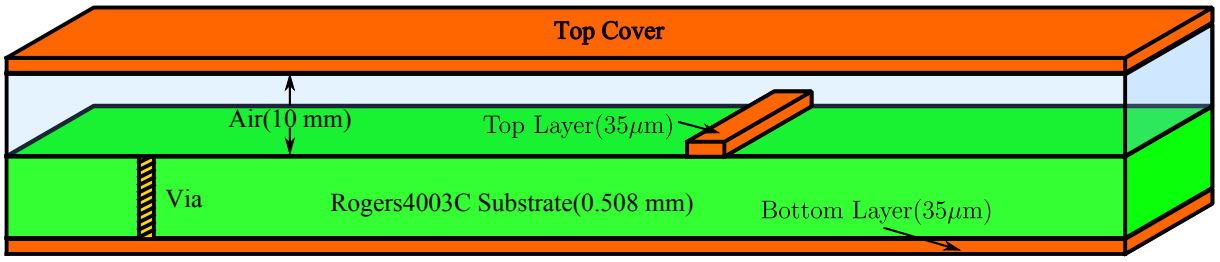


Figure 5.31: LNA Layer Distribution

The next stage after the EM-simulation is to use the EM data and co-simulate the LNA with ideal components for the matching networks on top of the layout. Optimization is needed because of the non unilateral nature of the transistor, since the isolation between the input and output of the amplifier is very good but not perfect, and the matching networks require some further adjustment. The optimization procedure used is the Newton search method which quickly moves to the first local minimum. Before the optimization process is started the following goals are set for the optimization algorithm in ADS

$$NF_{error} = |(NF - NF_{min})| \tag{5.6}$$

$$|S_{22}| < 20 \text{ dB} \tag{5.7}$$

$$|S_{21}| = 22 \text{ d}B \tag{5.8}$$

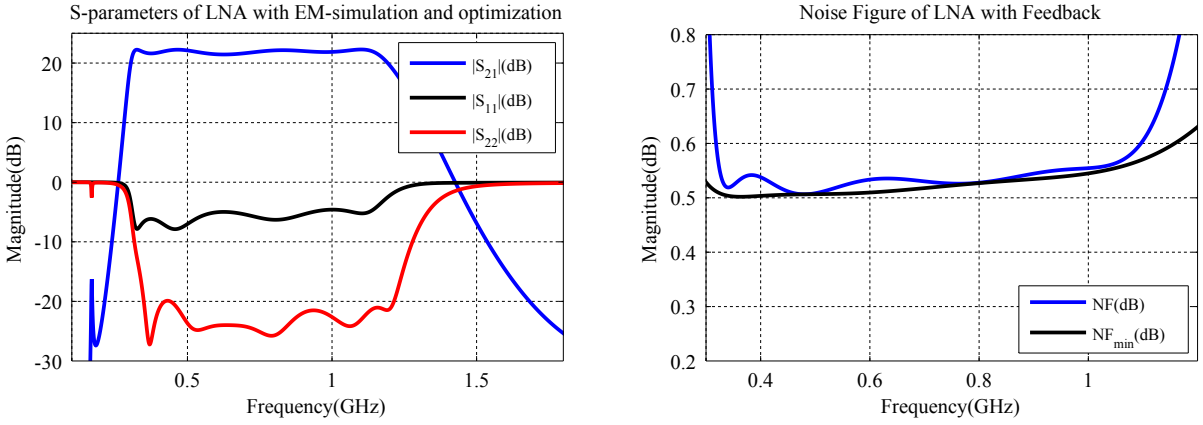
A simple optimization process is followed by starting with the noise matching section and defining the error function (5.6) and gain level (5.7), both goals are defined from 300 MHz to 1200 MHz. The starting values for the matching networks are shown in Table 5.9 and 5.10. Once the noise figure is minimized the attention shifts to the output matching network where the optimization

goals are set to (5.7) and (5.8) over the operation bandwidth. Thereafter, a final optimization step is executed which optimizes the input and output matching networks simultaneously using all three optimization goals minimum noise figure, output match and gain. The final optimized values for the matching networks of the LNA are shown in Table 5.11

Inductors:	L_2	L_3	L_4	L_5	L_6	L_7	
	80 nH	19 nH	37 nH	16 nH	14 nH	9.2 nH	
	L_{o1}	L_{o2}	L_{o3}	L_{04}	L_{o5}	L_{o6}	L_{o7}
	10 nH	14 nH	6.1 nH	4.5 nH	9.2 nH	16 nH	4.1 nH
Capacitors:	C_1	C_2	C_3	C_4	C_5	C_6	C_7
	100 pF	0.5 pF	39 pF	0.5 pF	39 pF	3.8 pF	6.4 pF
	C_{o1}	C_{o2}	C_{o3}	C_{o4}	C_{o5}	C_{o6}	C_{o7}
	5 pF	3.9 pF	6.7 pF	1.4 pF	7.2 pF	3.7 pF	13 pF

Table 5.11: Optimized element values for Matching Networks

The results of the S-parameters for the LNA with ideal matching networks are shown in Figure 5.32(a) and the blue line indicates that an excellent flat gain response is achieved above 20 dB with a 0.5 dB ripple across the operation bandwidth. The return loss from port 2 is equal to 20 dB as shown by the red line in Figure 5.32(a). S_{11} is equal to -5 dB across the frequency of interest which is an improvement compared to the amplifiers with no feedback.



(a) (b)

Figure 5.32: LNA results with EM-simulation and Optimization(a) S-parameters (b) Noise Figure

Figure 5.32(b) shows the noise figure of the overall LNA. As indicated by the blue line the NF is below 0.6 dB across the operation bandwidth. The noise figure starts to deviate rapidly from the minimum noise figure once the gain of the amplifier starts to decrease at the band edges. This attenuation in gain at the band edges increases the noise figure, when the definition of half power bandwidth is used to indicate the bandwidth of operation. The noise figure is therefore much higher than in the rest of the operation bandwidth.

The final stage in the design process is to incorporate component losses into the design. Vendor data from Coilcraft, Murata and Panasonic where used to be able to include the parasitic effects of each component in the design. The ideal components where replaced with 0402HP inductors from Coilcraft, GJM series capacitors from Murata and ERJ series resistors from Panasonic. According to the vendor data the components have low ESR values to reduce the amount of noise added by each component. The simulation results after adding the vendor components to the co-simulation set up are shown in Figure 5.33.

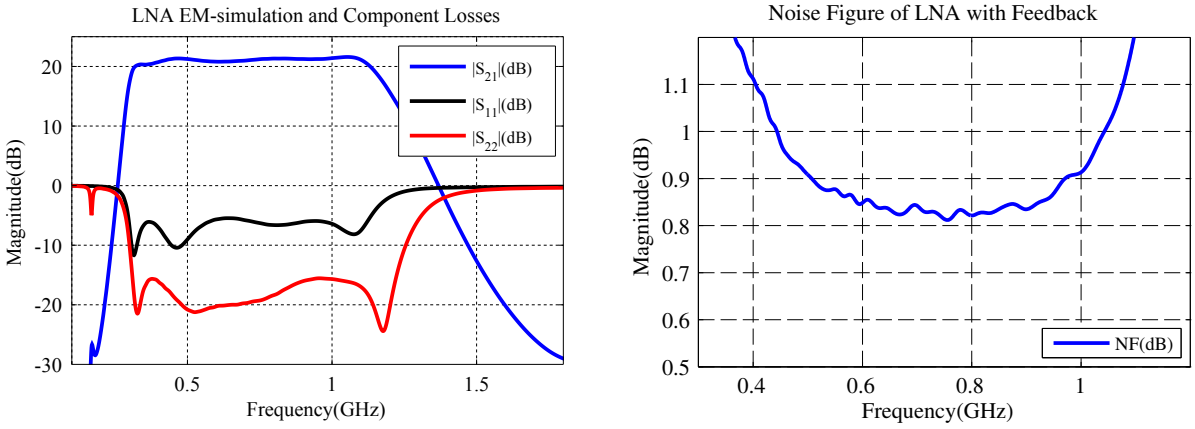


Figure 5.33: LNA results with component losses (a) S-parameters (b) Noise Figure

The influence of the component losses on the S-parameter results are shown in Figure 5.33(a). As indicated by the blue line, the gain of the amplifier remains above 20 dB and the ripple is only 0.5 dB across the operation bandwidth. The bandwidth narrowed slightly to 1.1 GHz because of possible weaker coupling between resonators due to the parasitic effects of the components.

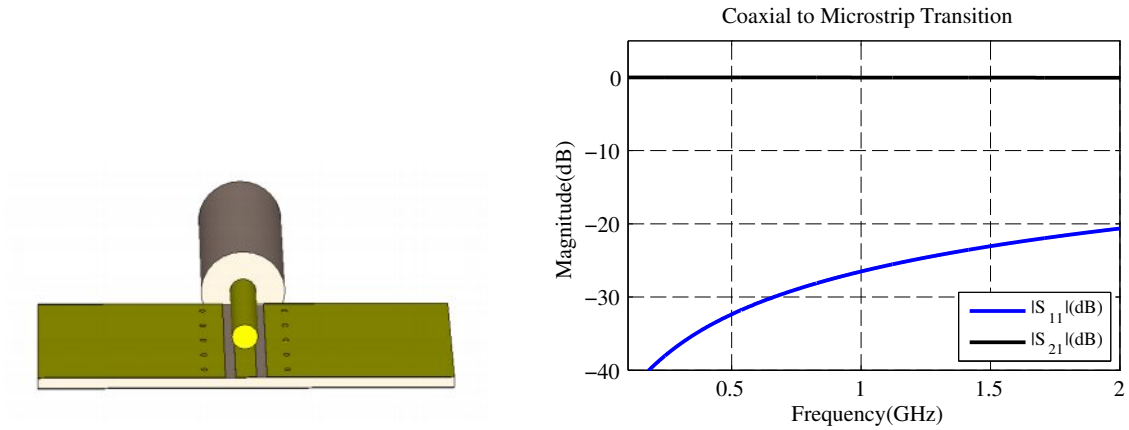
There is a big change in the output reflection as it shifts above -20 dB, but still remains below -15 dB across the operation bandwidth. The input reflection is still at -5 dB across the bandwidth, which is expected for minimum noise match for a 50 Ω system.

The noise figure of the LNA increased to 1.1 dB at the band edges and a minimum 0.85 dB is simulated at the centre of the operation bandwidth. A large increase in NF is due to the large matching networks used at the input of the device to achieve the desired match across the operation bandwidth. In wide band LNA design there is a constant trade off between bandwidth and NF because as the bandwidth increases the NF also increases.

5.4.4 Coaxial to Microstrip Transition

The connector that is chosen is a regular Huber + Suhner extended dielectric SMA (23-SMA-50-0-53) [42] with a 1.28 mm pin which fits adequately on the 1 mm wide microstrip feed lines shown

in Figure 5.30. Before the feedback amplifier is manufactured, the transition from the coaxial connector to the 50 Ω microstrip feed line is simulated in CST, as shown in Figure 5.34(a).



(a) (b)

Figure 5.34: Coaxial to microstrip transition (a) CST model (b) S-parameters

The results of the transition are shown in Figure 5.34(b), where the blue line indicates the input reflection coefficient S_{11} which is below -20 dB across the entire bandwidth of 350 MHz to 1200 MHz. Therefore the connector is a suitable choice for the LNA design and does not affect the performance.

5.5 Conclusion

This chapter presented four single stage low noise amplifiers. Starting with a single frequency design at 500 MHz which showed the lowest possible noise figure achievable of 0.6 dB for the technology chosen. The second design showed a wide-band LNA with no feedback from 300-600 MHz with excellent gain characteristics but a higher noise figure of 0.9 dB due to the large matching network at the input. If the bandwidth is extended even further to 900 MHz the gain level breaks down indicated by the large ripple in the passband and a high noise figure of 1.1 db is achieved. The final design included feedback which increased the complexity of the LNA. A high flat gain level is achieved equal to 20 dB with a minimum noise figure of 0.85 dB over a bandwidth of 350-1200 MHz. Measurements of the wide-band LNA with a feedback is shown in chapter 7.

Chapter 6

Multipath Amplifier Design

6.1 Problem Formulation

Traditionally amplifiers are designed to operate either in a single stage or cascaded configuration using sophisticated matching networks and negative feedback to achieve the wide-band performance as explained in chapter 5. A different approach of designing a wide-band LNA is demonstrated in this chapter, where the amplifiers are connected in parallel as shown in Figure 6.1 to form a multi-path low noise amplifier (MPLNA). The operation of the MPLNA is described as follows: where each path represents an amplifier operating at a single frequency f_1 to f_n and the goal is to amplify the intended signal with the corresponding path that operates at the same frequency and gets rejected by all the other paths operating at the other frequencies. All the different signals form various paths are superimposed at the output to give the intended wide band performance.

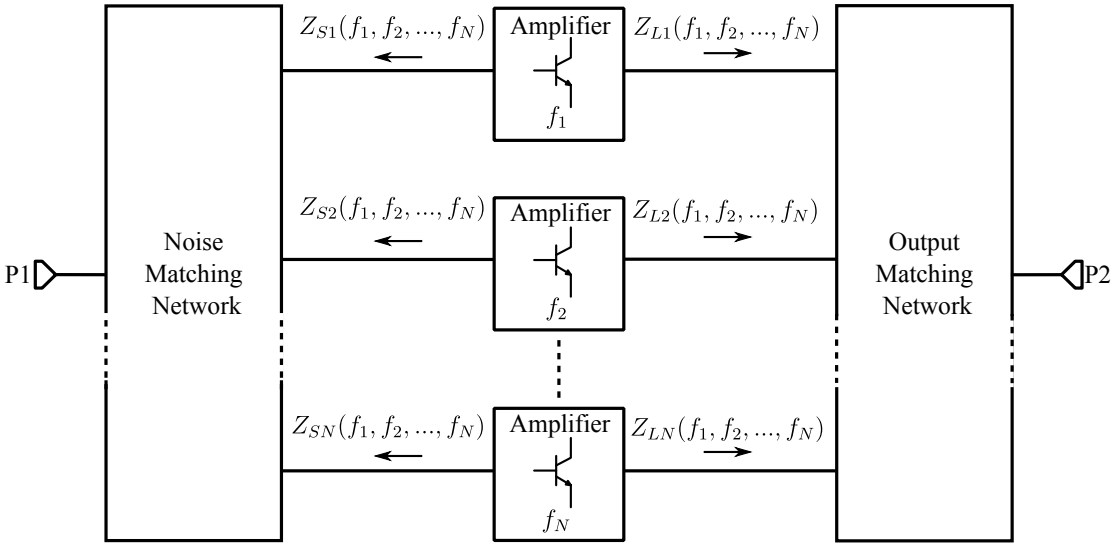


Figure 6.1: Multi-path LNA Configuration

Combining each stage in this manner reveals several problems, since each amplifier is matched for minimum noise and the optimum noise impedance Z_{opt} is different for each amplification path. This variation in Z_{opt} becomes a significant problem because each matching path is dependent

on the other. Mathematically the aim for each path can be written as

$$\begin{bmatrix} Z_{opt1}(f_1) \\ Z_{opt2}(f_2) \\ \vdots \\ Z_{optN}(f_N) \end{bmatrix} = \begin{bmatrix} Z_{S1}(f_1) \\ Z_{S2}(f_2) \\ \vdots \\ Z_{SN}(f_N) \end{bmatrix} \tag{6.1}$$

where the goal is to match each input path Z_{S1} to $Z_{Z_{SN}}$ the optimum noise impedance Z_{opt1} to Z_{optN} at the specified operating frequency. It is important to note that each path is interlinked with the other and to arrive at a closed form solution for each input path is impossible since each input impedance is dependant on the other impedances seen from each port.

The same problem arises at the output of the MPLNA where all the different paths are linked together and mathematically written as,

$$\begin{bmatrix} Z_{out1}(f_1) \\ Z_{out2}(f_2) \\ \vdots \\ Z_{outN}(f_N) \end{bmatrix} = \begin{bmatrix} Z^*_{L1}(f_1) \\ Z^*_{L2}(f_2) \\ \vdots \\ Z^*_{LN}(f_N) \end{bmatrix} \tag{6.2}$$

where Z_{out} is the output impedance for each path seen from port 2 at each operating frequency and Z_L is the corresponding load impedance for each path. Another difficulty with this type of structure is to keep the design of the input and output matching networks separate. The BFP842 transistor that is used for this design has a very small S_{12} (see appendix A) but is not equal to zero, which indicates that there are some level of interaction between the input and output matching networks. If the amplifiers are connected in parallel this small interaction between every input and output path complicates the design process even further and an optimization algorithm is necessary in order to consider all the effects at once.

For a proof of concept a two stage multi-path design is developed to achieve a minimum noise figure at $f_1 = 500$ MHz and $f_2 = 700$ MHz. The output network is matched for maximum power transfer for a 50 Ω system and the same transistor is used as in the single stage designs to compare the design technique with that of chapter 5. A final multi-port noise analysis is done to be able to compare the noise figure calculated by the simulation software and that based on the multi-port noise theory discussed in chapter 2.

6.2 Design Process

6.2.1 Single Frequency Amplifier Design

The design process of the MPLNA starts with designing two single stage LNA's to operate at $f_1 = 500$ MHz and $f_2 = 700$ MHz. Following the design procedure described in section 5.1, where both low noise amplifiers are biased at $V_{ce} = 2.5$ V and $I_c = 5$ mA. Using the stability and biasing configuration described in section 5.1.1 to achieve the lowest possible NF at the operating frequencies. A schematic of each LNA are shown in Figure 6.2,

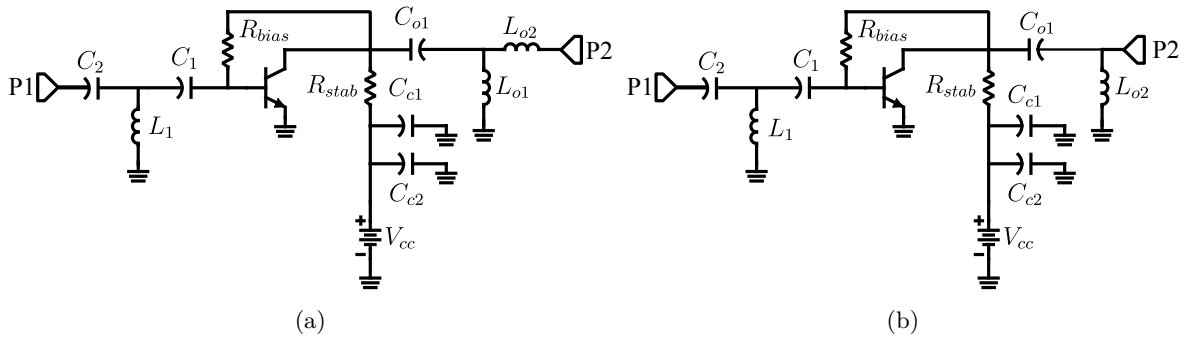


Figure 6.2: Single Frequency LNA (a) 500 MHz (b) 700 MHz

where the matching networks for each LNA are determined, using the graphical Smith chart approach as described in section 5.1.2. The element values for the amplifiers are shown in Table 6.1.

Inductors:	L_1	L_{01}	L_{02}
	22 nH	112 nH	7.37 nH
Capacitors:	C_1	C_2	C_{o1}
	47 pF	4.3 pF	26.5 pF
Resistors:	R_{bias}	R_{stab}	
	105 kΩ	60 Ω	

(a)

Inductors:	L_1	L_{01}	
	16 nH	22.56 nH	
Capacitors:	C_1	C_2	C_{o1}
	47 pF	1.5 pF	60 pF
Resistors:	R_{bias}	R_{stab}	
	105 kΩ	60 Ω	

(b)

Table 6.1: Element values of Single Frequency LNA's:(a) 500 MHz (b) 700 MHz

6.2.2 Wilkinson Power Divider

A Wilkinson power divider is added to the output of the MPLNA to create isolation between the output ports of each path. This gives the designer the freedom to directly couple the output of each amplification path to the Wilkinson divider and minimizes the loading effect each output path has on each other. The same method can not be used at the input of the MPLNA to isolate each path from each other because the isolation resistors of the Wilkinson power divider adds unwanted noise to the input which increases the overall noise figure of the receiver system. A circuit schematic of the Wilkinson power divider is shown in Figure 6.3
It is required that the power divider operates from 400 - 800 MHz since we want to ensure that both frequency paths are covered. A two stage Wilkinson power divider are selected because adding an extra stage in the design increases the bandwidth of the divider to achieve the desired response, since a single stage design operates over a very narrow bandwidth. The main specification of the power divider is to provide at least 20 dB of isolation between the output ports and have a power match below 15 dB at each port. An operating frequency of 600 MHz is chosen with a Chebychev equal ripple approximation to achieve the wider band response.

The impedance for each quarter wave section of the power divider are determined by bisecting the circuit shown in Figure 6.3 into its even and odd mode presentations. For the even mode

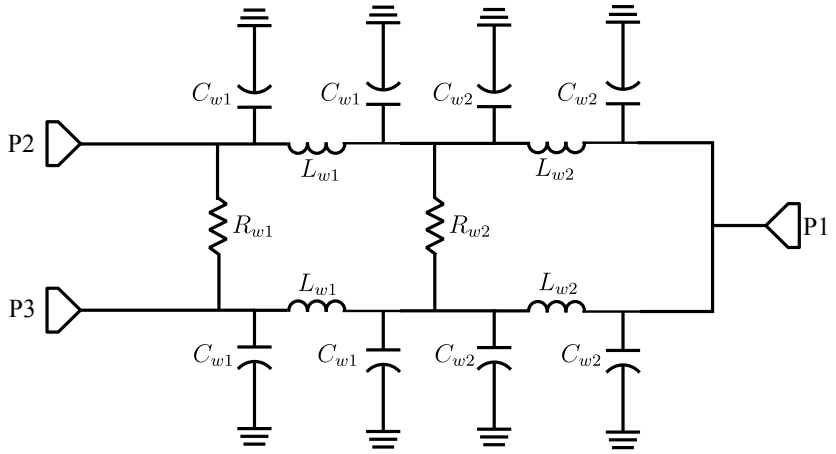


Figure 6.3: Wilkinson power divider for output matching

presentation the resistors are ignored because of the open circuit ends connected to each resistor therefore no current can pass through the resistors. Port 1 is split up into two equal 100 Ω resistors to analyse each presentation separately. This leaves a simple calculation of each section using the multi section transformer techniques derived in [22] to match a 100 Ω load to a 50 Ω source. The impedance for the two sections are determined to be equal to $Z_1 = 82$ Ω and $Z_2 = 60$ Ω. The isolation resistors are determined by using the optimizer in ADS and setting the isolation between port 2 and 3 below -20 dB from 400 MHz to 800 MHz and the final results of the resistors are shown in Table 6.2

An equivalent lumped element circuit are derived for each transformer section in [43], since using classic transmission lines for each section are impractical, since a quarter wavelength at 600 MHz are equal to 77 mm when using a microstrip line with a Rogers 4003C substrate with a thickness of 0.508 mm. The results after converting from one presentation to another are shown in Table 6.2.

Inductors:	L_{w1}	L_{w2}
	15 nH	20 nH
Capacitors:	C_{w1}	C_{w2}
	2.7 pF	2.7 pF
Resistors:	R_{w1}	R_{w2}
	176 Ω	106 Ω

Table 6.2: Calculated values for Wilkinson Power Divider

A layout of the Wilkinson power divider is created in ADS and a full wave EM-simulation is performed to take into account the extra coupling added between components caused by the added inductance of track lengths between the different elements and the capacitance to ground from the top and bottom layers. The final results of the Wilkinson power divider are shown in Figure 6.4 and the blue line indicates the power transferred from port 1 to 2 and is equal to -3 dB across the operation bandwidth. The reflection from port 1 is below -15 dB from 350 MHz to 750 MHz shown by the black line. The red line indicates an excellent power match from port

2 as the reflection coefficient is equal to 20 dB from 400 to 750 MHz. As indicated by the cyan line, the isolation between ports 2 and 3 is equal to 19 dB at the centre frequency and are well below 20 dB at the two operating frequencies of the MPLNA. The other port combinations are not showed in Figure 6.2, due to the symmetry of the structure.

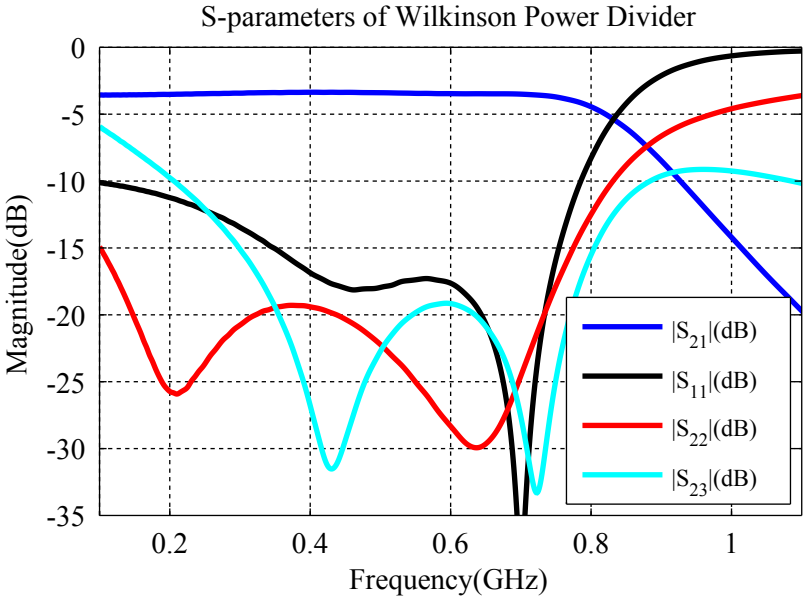


Figure 6.4: Wilkinson power divider for output matching

6.2.3 Noise Compensation Network

The next step in the design procedure is to add noise matching compensation networks to the input of the MPLNA. The function of the compensation networks is to minimize the influence of the different signal paths on each other. This enables the MPLNA to have a minimum noise match for each amplifier according to its operation frequency. Classic matching techniques can not be used because adjusting the one path for optimum noise corrupts the noise match of the other path.

A solution to the problem is to use different optimization schemes in ADS and Matlab to determine possible configurations for the compensation networks by trial and error. Starting with adding only a single element either an inductor or capacitor to each path and optimizing to minimize the influence. The optimization approach assumes that the transistor is unilateral and that the amplifier is modelled with a single impedance Z_{L1} and Z_{L2} at the input port of each transistor as shown in Figure 6.5(a).

A matlab script is written which uses the fmin search function to find the minimum for the input impedance $Z_{in1}(f_1)$ and $Z_{in2}(f_2)$ seen from the individual transistors as shown in Figure 6.5(a). The error function used for the minimum noise optimization for both signal paths can be written

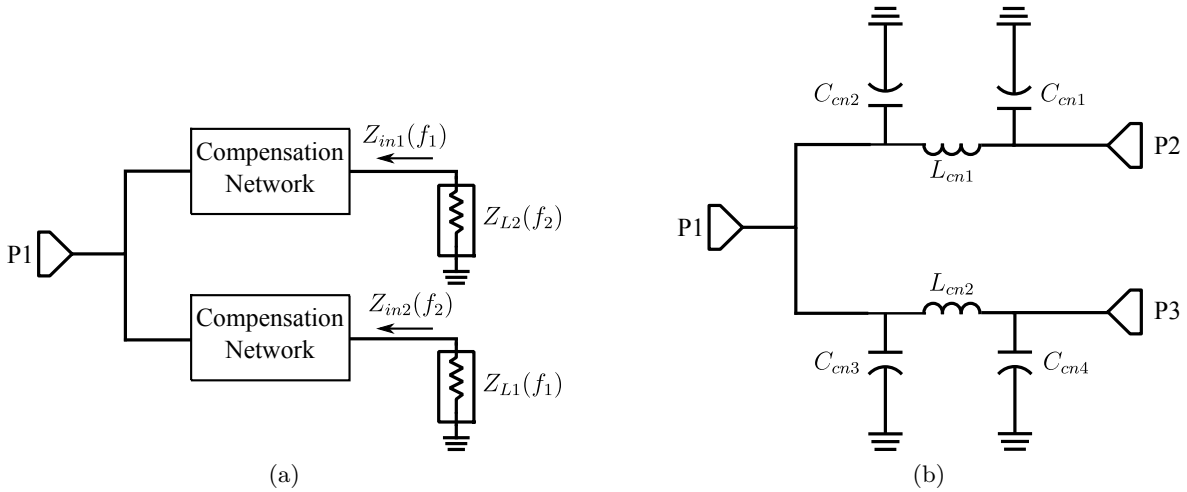


Figure 6.5: Compensation network optimization (a) Modelled topology (b) Optimal circuit

as

$$Z_{error} = |Z_{in1}(f_1) - Z_{opt1}(f_1)| + |Z_{in2}(f_2) - Z_{opt2}(f_2)| \tag{6.3}$$

where $Z_{opt1}(f_1)$ and $Z_{opt2}(f_2)$ are the optimum noise impedance for each amplifier at the operating frequency of each path. The challenge in using the fmin search optimization scheme is that the optimizer gets stuck in a local minimum depending on the starting value of the individual elements of the compensation network. In order to overcome this problem the starting values for each element are swept from 1 to 100 pF for the capacitors and from 1 to 200 nH for the inductors.

It is important to note that there are multiple solutions to this optimization problem and in certain cases the solution of the elements of the compensation network are negative. Indicating that either it is not possible to manufacture the configuration selected or the current element needs to be replaced with an inductor or capacitor depending on the starting value of the element. After numerous iterations of optimization the final circuit is shown in Figure 6.5(b) and the values for the circuit are shown in Table 6.3

Inductors:	L_{cn1}	L_{cn2}		
	21 nH	11.4 nH		
Capacitors:	C_{cn1}	C_{cn2}	C_{cn3}	C_{cn4}
	5 pF	4.8 pF	1.1 pF	1 pF

Table 6.3: Optimized values for compensation networks

6.3 EM-simulation and Optimization

A final step in the design procedure is to realise the theoretical design by performing a full-wave EM-simulation with ADS. Connecting the individual parts from each section does not yield an optimal result, since the transistors are not perfectly unilateral. Further optimization is needed to account for all the interactions between the two input paths as well as the effect of the input

and output matching networks on each other.

The layout of the multi-path LNA is shown in Figure 6.6, where great care is taken to minimize the track length between components in order to reduce the added inductance between components. The layout is done on a Rogers 4003C substrate [41] with a thickness of 0.508 mm and the height of the copper cladding is chosen equal to 0.35μm. A closed box environment selected as for the feedback amplifier in section 5.4 with a height of 10 mm in order to shield the MPLNA from any unwanted signals which degrades the noise figure performance of the device.

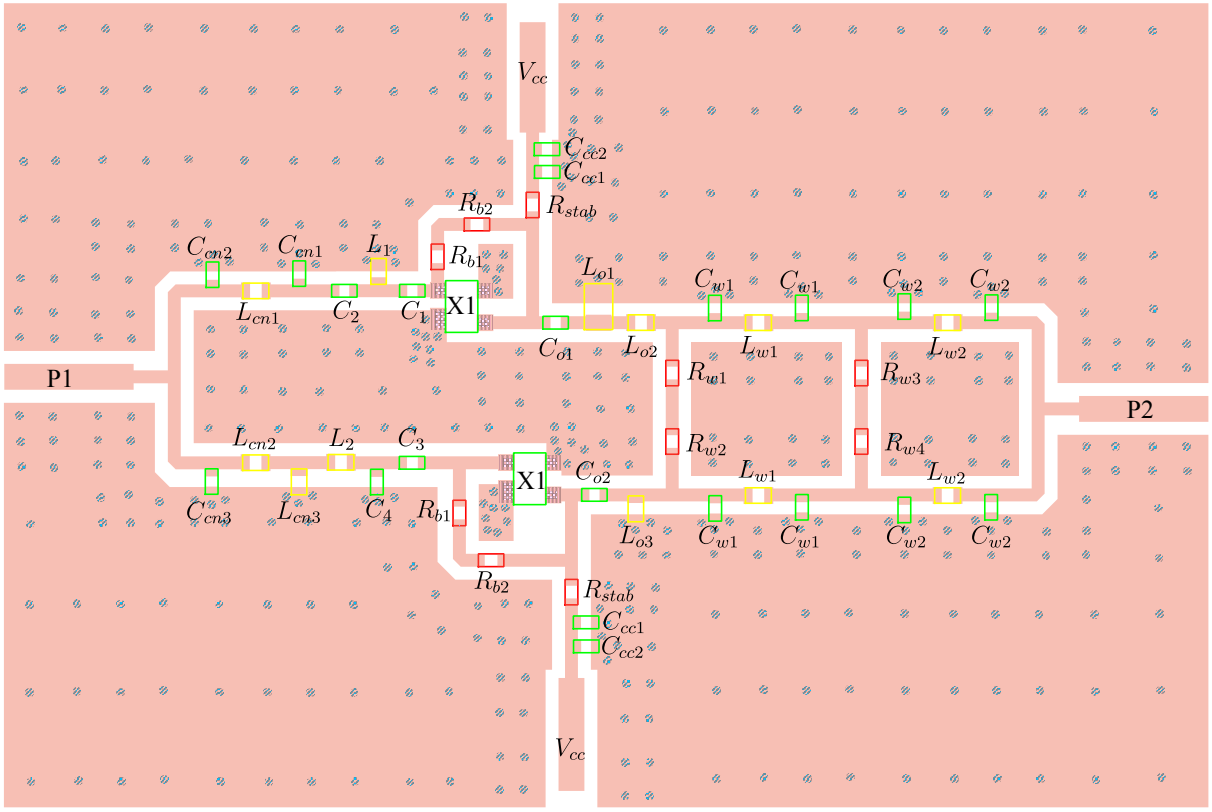


Figure 6.6: Multi-Path LNA Layout

A co-simulation is performed with ideal components on top of the PCB layout shown in Figure 6.6. The optimization goals are set as

$$NF_{error} = |NF_{multipath} - NF_{min(transistor)}|, \text{ at } f_1 \text{ and } f_2 \tag{6.4}$$

$$|S_{22}| < -15dB \text{ at } f_1 \text{ and } f_2 \tag{6.5}$$

First the input compensation networks are optimized to achieve a minimum noise figure at f_1 and f_2 using a global optimization search method in ADS. Using the global search method does increase the optimization time and it takes the solver a significant amount of time to do each iteration when the co-simulation is performed with the EM-simulation data. After optimizing for minimum noise the next step in the optimization algorithm is to adjust the output matching networks because adjusting the input network affected both output networks for each signal path. A Newton search method is applied only adjusting the single matching elements at the

output of each path for a minimum output reflection coefficient as described by equation (6.5). The solver quickly adjusted the output matching networks to reach the desired goal only after a few iterations.

The final step in the optimization process is to simultaneously optimize the input and output matching using the Newton search method. Using this optimization scheme after the global search proved to work more effectively, since the answer is closer to an optimal solution. The same goals as described by equation (6.4) and (6.5) are used and it is found that the input network needs adjusting by replacing the capacitor C_{cn4} with an inductor L_{cn3}, due to the value of the capacitor becoming impractical and an improved noise match is obtained by adding L_{cn3}. The final optimized values for the MPLNA are shown in Table 6.4.

Inductors:	L_1	L_2	L_{cn1}	L_{cn2}	L_{cn3}		
	27 nH	16 nH	20 nH	7.5 nH	40 nH		
	L_{o1}	L_{o2}	L_{o3}	L_{w1}	L_{w2}		
	110 nH	7.5 nH	22 nH	15 nH	20 nH		
Capacitors:	C_1	C_2	C_3	C_4	C_{cn1}	C_{cn2}	C_{cn3}
	47 pF	4.3 pF	47 pF	1.5 pF	2.7 pF	1 pF	4.3 pF
	C_{o1}	C_{o2}	C_{w1}	C_{w2}	C_{cc1}	C_{cc2}	
	27 pF	56 pF	2.7 pF	2.7 pF	3300 pF	22000 pF	
Resistors:	R_{stab}	R_{b1}	R_{b2}	R_{w1}	R_{w2}	R_{w3}	R_{w4}
	56 Ω	100 kΩ	5.6 kΩ	100 Ω	5.6 Ω	120Ω	56 Ω

Table 6.4: Optimized element values for Multi-Path Design

After the optimization is completed the ideal components are replaced with vendor supplied components to analyse how the noise is influenced by the component's parasitic effects. The vendors that are used is Murata 0402GJM series for the capacitors, Coilcraft 0402HP series for the inductors excluding one 0602HP component for the 110 nH inductor and Panasonic for the 0402 resistors. The final results of the EM-simulation with component losses are shown in Figure 6.7.

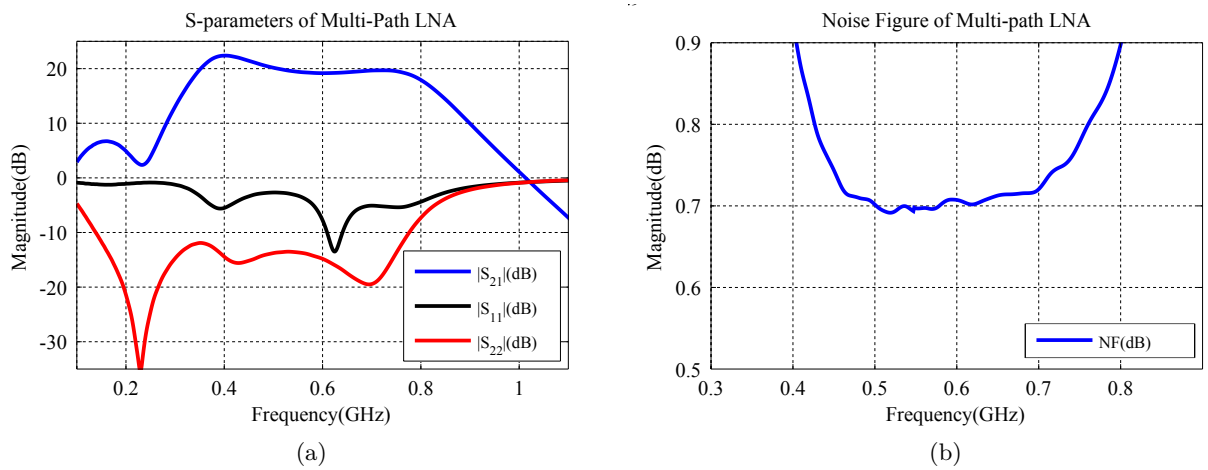


Figure 6.7: Results of Multi-Path LNA with component losses (a) S-parameters (b) Noise Figure

As shown in Figure 6.7(a) the gain at both frequencies $f_1 = 500$ MHz and $f_2 = 700$ MHz are equal to 20 dB as indicated by the blue line. The output reflection coefficient S_{22} shown by the red line is equal to 14 dB at 500 MHz and equal to 19 dB at 700 MHz which indicates that the total power is transferred excellently to the output port.

The noise figure of the Multi-Path LNA is shown in Figure 6.7(b), where the noise figure is equal to 0.72 dB from 500 to 700 MHz indicated by the blue line. There is a significant band-width improvement when using this type of configuration compared to just the classic single frequency response as shown in section 5.1. Also the noise figure obtained over a 200 MHz bandwidth is 0.2 dB lower than the single stage design from 300-600 MHz showed in Figure 5.23(b). The disadvantage is that the complexity is increased significantly and EM-simulation software is required to obtain an accurate result.

6.4 Multi-port Noise Analysis

The purpose of this section is to use the multi-port theory described in section 2.6 to analyse the multi-path amplifier and compare the theoretical noise figure to the simulated NF shown in Figure 6.7 (b). Starting with dividing the multi-path amplifier into its active and passive part as shown in Figure 6.8, where the passive part consists of the input and output matching sections and the active part is the two port transistor data with noise parameters.

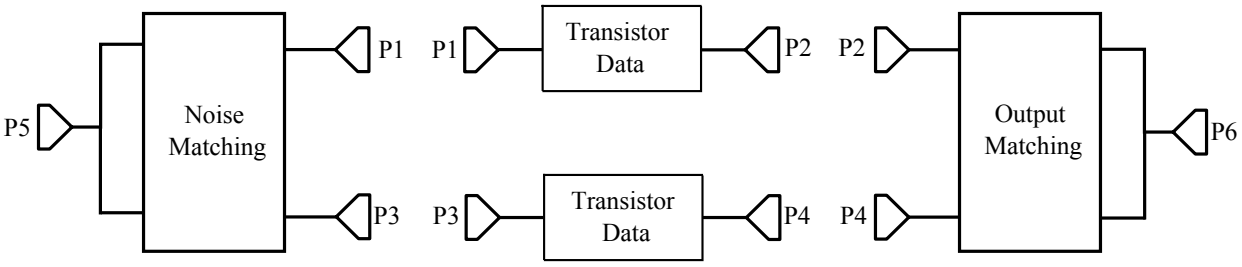


Figure 6.8: Multi-Path LNA Layout

According to equation (2.107) the noise correlation matrix for the entire multipath amplifier is written as

$$[C_s] = [H_N][C_N][H_N]^\dagger + [H_J][C_J][H_J]^\dagger \tag{6.6}$$

where $[C_J]$ is the correlation matrix from the transistor data derived from the noise parameters as shown by equation (2.71). The noise correlation matrix of the passive structure $[C_N]$ is determined by using equation (2.63) assuming that all the noise generated by the passive structure are thermal in nature.

The matrices $[H_N]$ and $[H_J]$ are calculated according to equation (2.100) and (2.98) and it is very important to structure the [Y] matrix correctly, which is partitioned according to the

internal(d) and external(e) ports as follows

$$[Y] = \begin{bmatrix} y_{dd} & y_{de} \\ y_{ed} & y_{ee} \end{bmatrix} \tag{6.7}$$

where ADS is used to simulate the entire broken up parts individually to determine the [Y] matrix. Once the Y-matrix is partitioned correctly $[C_s]$ is determined through a computational program for example matlab. The final step in the theoretical calculations is to calculate the noise figure of the MPLNA by using equation (2.86) and the results of the theoretical calculations compared to the ADS simulation are shown in Figure 6.9

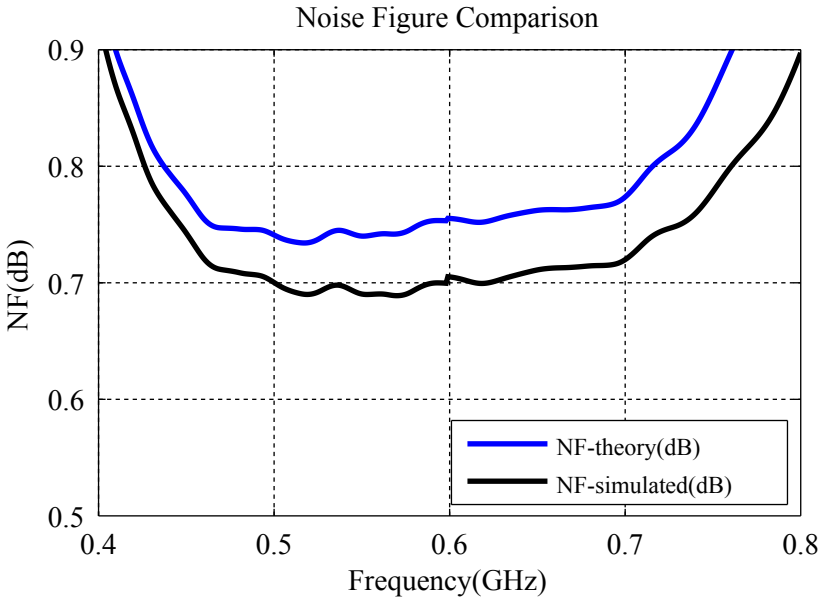


Figure 6.9: Multi-Path LNA Layout

The theoretical noise figure calculated by matlab indicated by the blue line agrees well with simulated noise figure in ADS as shown by the black line in Figure 6.9. A small deviation of 0.05 dB is reached between the simulated and theoretical calculations. There is also a difference in the models used to determine the noise contribution of the active part where, ADS used a spice model generating the noise data at each frequency and in the theoretical calculations the noise parameter data provided by the vendors is used for the theoretical calculations. Overall the agreement between the theoretical calculation and simulated values shows that the noise figure of a multi-port structure is analysed accurately by using classical multi-port noise theory.

Chapter 7

Measurements and Results

7.1 Different Types of Noise Measurements

7.1.1 Y-factor Method

The Y-factor method consists of making two noise power measurements using a known noise source characterised by its Excess Noise Ratio (ENR). A noise source usually contains a diode and when this diode is reversed biased and driven into avalanche breakdown mode it creates a jolt of noise at the output port of the noise source. This excess noise generated by the diode is commonly referred to as the hot measurement. In its cold state the diode creates thermal noise at the output port and since the diode admittance is proportional to the bias current there is significant difference in the source admittance of the hot and cold measurements [44].

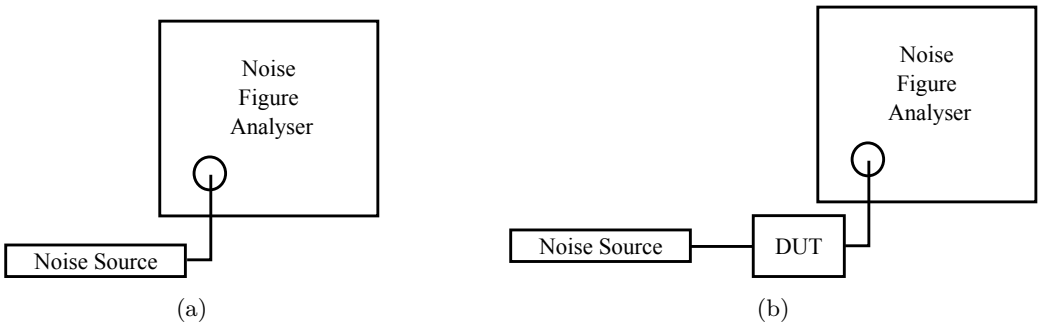


Figure 7.1: Y-factor Measurement Process (a) Calibration (b) Measurement

The results of the hot and cold states are used to determine two variables, the gain G_T of the amplifier and the noise figure NF. Figure 7.2 shows the measurement process of the Y-factor method. First the noise source is directly connected to the noise figure analyser (NFA) to characterize the noise generated by the NFA's internal network as shown in Figure 7.1 (a). Next the device under test (DUT) is connected between the noise source and the NFA as shown in Figure 7.1(b) a hot and cold measurement is now performed to determine the noise characteristics of the device. It is important to note that the noise source is involved in both steps, calibration and measurement, which differs from the cold source method explained later in section 7.1.2.

Behind the scenes the NFA uses the hot and cold measurements to determine the desired variables G_T and the Y-factor Y_f as shown in Figure 7.2

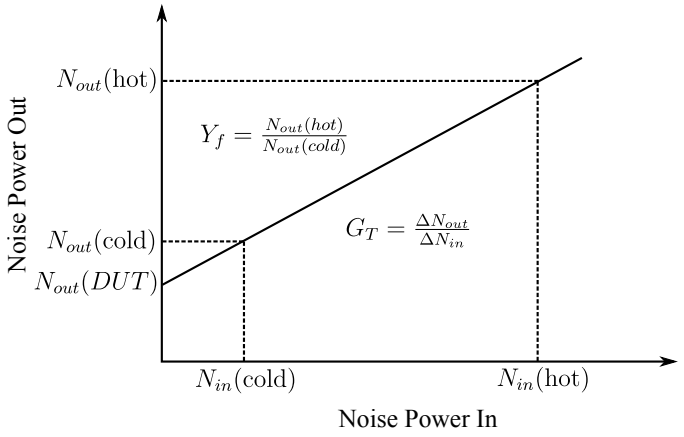


Figure 7.2: Graphical representation of Y-factor method

The Y-factor measurement is dependent on the linearity of the device and for low noise amplifiers this is usually a good assumption, since the LNA operates far from the compression region of the amplifier and only amplifying very small signals. From this linear ratio G_T is calculated from the slope of the output powers measured from the device under test (DUT). The noise factor of the total measuring system including the NFA and DUT is calculated as follows [45]

$$F_{sys} = \frac{ENR}{Y_f - 1} \tag{7.1}$$

where the ENR values is used from the noise source and Y_f is calculated by measuring the hot and cold noise powers at the NFA. The noise factor of the DUT is determined by using Frii's noise equation of a cascaded system [18]

$$F_{1(DUT)} = F_{sys} - \frac{F_{2(cal)} - 1}{G_T} \tag{7.2}$$

where F_2 is determined from the calibration step and G_T is derived from the slope of the hot and cold measurement as explained earlier.

7.1.2 Cold Source Method

The cold source method consists of measuring the output noise power from the DUT with a cold source termination at the input. With this given information the measuring system calculates the system noise factor as follows [45]

$$F_{sys} = \frac{N_{out}(\text{cold})}{kT_0 \Delta f G_T} \tag{7.3}$$

where G_T is the gain of the amplifier, Δf is the noise bandwidth of the measuring system, k is Boltzmann constant and $T_0 = 290$K standard room temperature in kelvin. It is important to note than when using the cold source technique a very high accuracy gain measurement is needed in order to obtain accurate results. This is why the technique is usually used in co-junction with vector network analysers (VNA). The measurement setup of such a system is demonstrated in

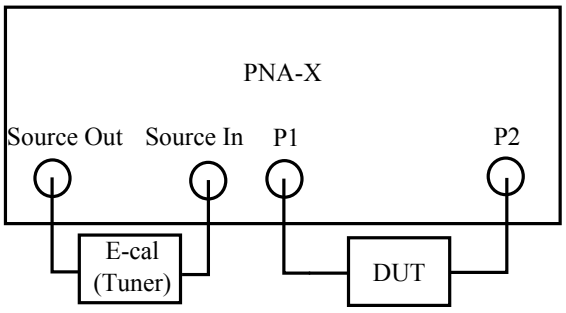


Figure 7.3: Cold source Measurement Setup with PNA-X

Figure 7.3.

A calibration step is required just as in the Y-factor case where a noise source is connected to port 2 in Figure 7.3to be able to characterize the noise generated by the measuring system. There after the DUT is connected between port 1 and 2 and the output noise power can be measured.

Also shown in Figure 7.3 is an E-cal(electronic calibration) module which as available with the Agilent PNA-X series used for this project. This E-cal module serves as an impedance tuner to help with possible source mismatches that can occur. It adjust the source impedance to four different known impedances and then the average of the output noise power is taken to acquire a more accurate result. The E-cal module needs to be connected before the calibration process is started. This setup also have the advantage of simultaneously measuring the S-parameter data of the device. The S-parameter data is used for the gain calculations which is used to accurately determine the noise figure of the device.

Another advantage of this measurement setup is to be able to replace the E-cal module which can only be used for a 50Ω system with a complete impedance tuner. This impedance tuner is used to fully characterize the noise characteristics of the device for any impedance level.

7.1.3 Comparison of Y-factor and Cold-Source Method

In order to compare the two measurement techniques both measuring systems where setup as explained in section 7.1.2 and 7.1.1. The device under test is the wide-band LNA with feedback designed in chapter 5, where the same 6 dB noise source (Agilent 346C) is used in both measurements. The goal is to measure a NF at 1.2 dB according to the simulation results. The results of both measurements are shown in Figure 7.4 where, the black line indicates the Y-factor method and the red line the cold source method. The noise figure of the Y-factor varies significantly over the frequency range of 350 MHZ to 1.2 GHz. This is due to the drastic change in the source admittance from the hot and cold state. It is important to note that when designing a wide band amplifier it is very difficult to precisely match the amplifier across the frequency range to 50 Ω source.

The cold source method shows a much more conclusive result. As the PNA-X measurement system includes an E-cal module to be used for a tuner. The result of averaging the four measurements taken at four different impedance levels decreases the uncertainty of the measurement. The prefered method is the cold source method, since the S-parameter measurements is also done by the PNA-X and reduces setup time.

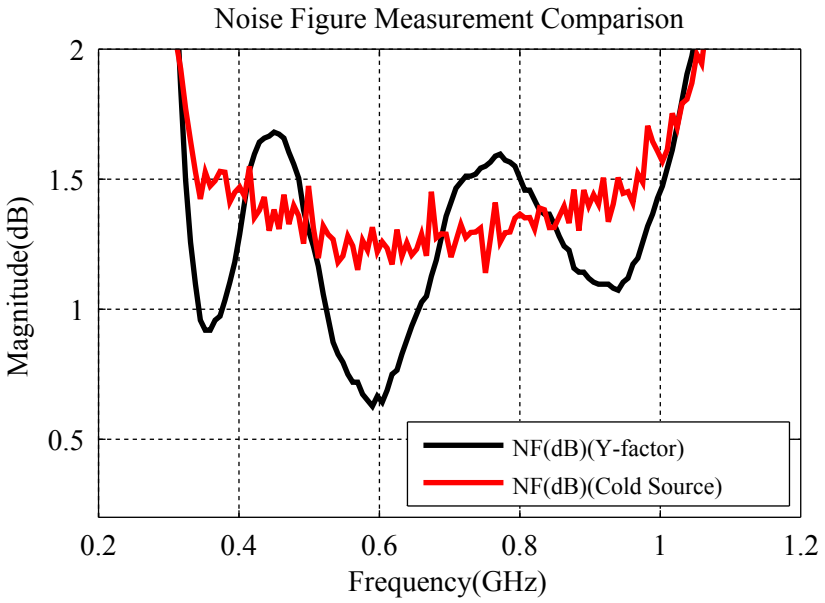


Figure 7.4: Comparison of Y-factor and Cold Source Method

7.2 Results of Wide-Band LNA (350-1200 MHz)

The wide-band LNA with feedback designed in chapter 5 is fabricated and shown in Figure 7.5. The PCB is fabricated at TRAX using a Rogers 4003C substrate with a height of 0.508 mm. The RF enclosure is made at Stellenbosch University and the components is soldered on by hand at the work shop at Stellenbosch University. The total size of the PCB is 25 mm by 55 mm making it quite large due to the matching networks needed to obtain the wide-band performance.

The PNA-X(N5242A) that uses a cold source method as explained in section 7.1.2 to calculate the noise figure and S-parameters of the device simultaneously is used to measure the performance of the LNA. The S-parameter results of the wide-band LNA are shown in Figure 7.6, where the dotted lines represents the ADS simulations and the constant lines indicates the measurements. As shown by the blue line in Figure 7.6 the gain of the amplifier agrees well with the simulated values and drops just below 20 dB at the higher frequencies. The cause of this deviation could be because the output match indicated by the red line in Figure 7.6 which have a 5 dB difference between the simulated (dotted magenta line) and the measured value. A big variation in the output match could be because of component mismatches in the output network causing more reflection at the output port. The values of the component can not be

identified since very small 0402 components are used and it is difficult to determine where the exact mistake occurred.

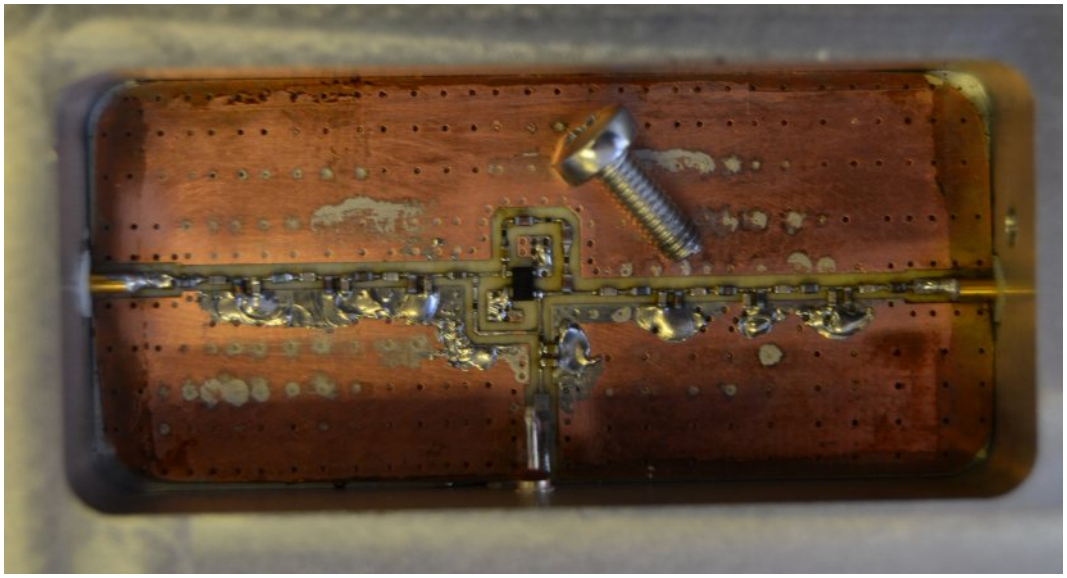


Figure 7.5: Fabricated Wide-Band LNA (300-1200 MHz)

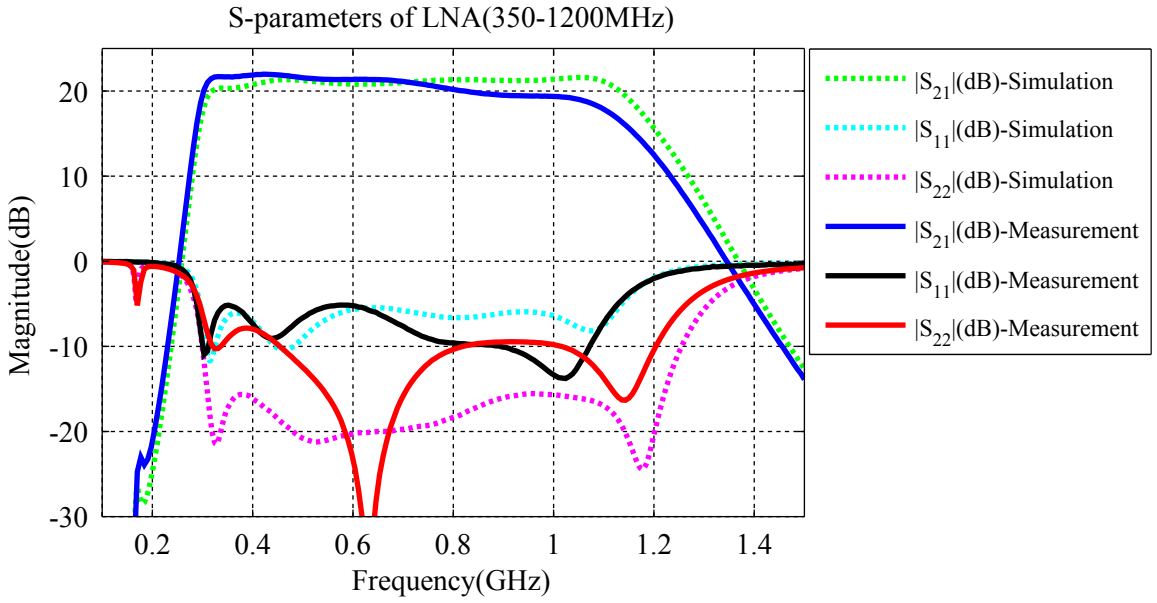


Figure 7.6: S-parameter Results of Wide-Band LNA (300-1200 MHz)

The input reflection coefficient agrees well with the simulated values at the lower frequencies and deviates slightly from the simulated values at the higher frequencies. This could again be because of component tolerances since some of the components deviate about 5 % from the original value and could cause a mismatch.

The noise figure of the LNA are shown in Figure 7.7 the measured value of the LNA is below 1.5 dB across the band of interest. The reason why the NF is higher is because in the simulated values the noise generated by the SMA connectors are not included in the design. The SMA connectors used typically adds about 0.2 dB to the noise figure which means there is about a 0.2 dB difference in the expected noise figure. This again could be because of the mismatch in the output network causing a decrease in the gain resulting in a higher noise figure.

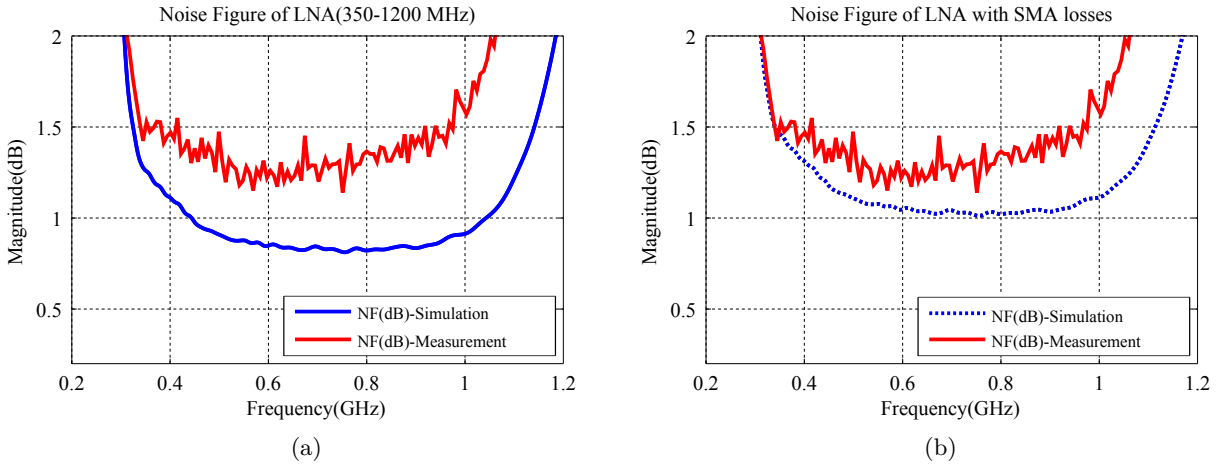


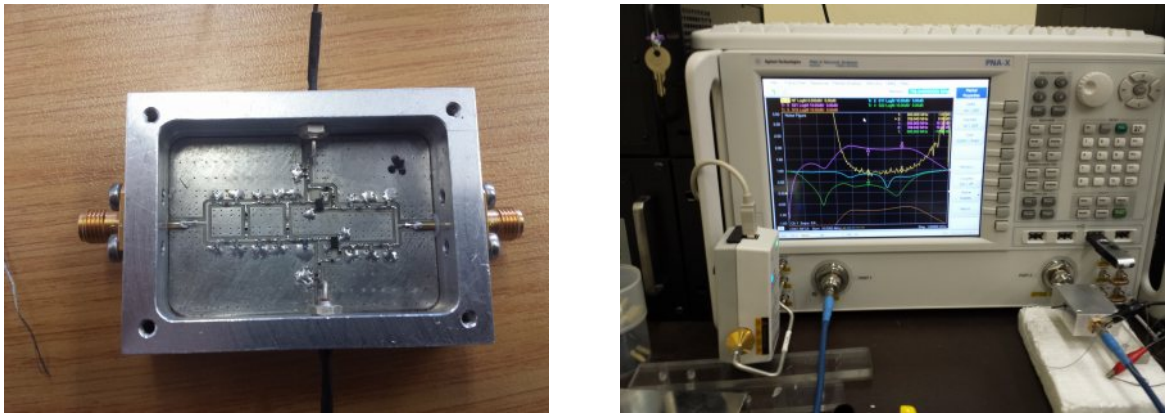
Figure 7.7: Noise Figure of Wide-Band LNA:(a)Simulation vs Measurements (b)SMA losses included in Simulation

7.3 Results of Multi-Path LNA

The Multi-Path LNA developed in chapter 6 is fabricated and the result of the fabrication process is shown in Figure 7.8(a). The PCB of the multi-path LNA is manufactured at TRAX and the RF enclosure and component placement is done at Stellenbosch University. Measuring the MPLNA is done with the PNA-X noise measurement system as shown in Figure 7.8(b), where a cold source measurement technique was implemented as discussed in section 7.1.2.

A 4 MHz noise bandwidth is selected and an input power level of -40 dBm. The total amount of sample points is 201 across the operation bandwidth. A narrower noise bandwidth can be selected but this increases the measuring time and sufficient results are obtained using the 4 MHz bandwidth. The final measured S-parameter results are shown in Figure 7.9 by the solid lines. Excellent agreement is achieved with the simulated values indicated by the dotted lines.

As shown in Figure 7.9 the blue line indicates the gain of the amplifier and the desired gain at 500 MHz is equal to 19.2 dB and almost the same level is measured at 700 MHz where the gain of the amplifier is equal to 19.3 dB. The measured output reflection coefficient S_{22} indicated by the red line is in good agreement with the simulated values and only deviates at 0.6 GHz, this could be due to component tolerances that is not perfectly included in the simulation.



(a) (b)

Figure 7.8: Multi-Path LNA (a) Fabricated (b) Measurement setup

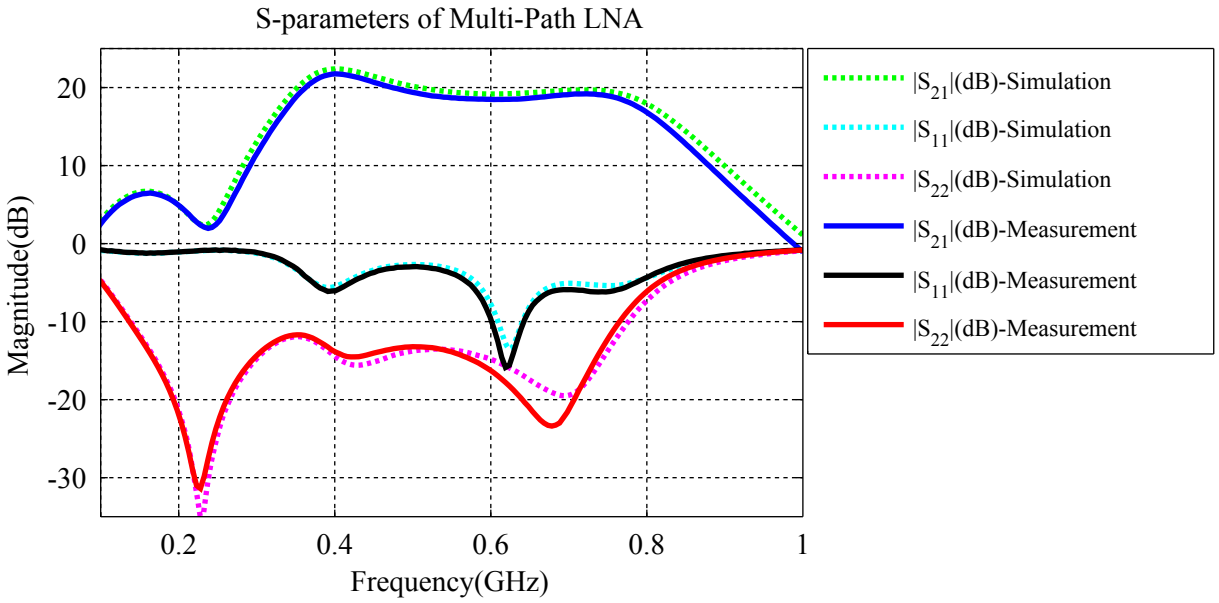


Figure 7.9: S-parameter Results of Multi-Path LNA

The input reflection coefficient indicated by the black line corresponds well to the simulated values where the weaker input match is due to the fact that we matched for minimum noise and not for maximum power transfer. A closer look at the noise measurements results of the MPLNA as shown in Figure 7.10(a) indicates a 0.2 dB difference between the measured noise figure indicated by red line and the simulated noise figure shown by the dotted blue line.

The 0.2 dB difference is there because the noise generated by the SMA connectors was not included in the simulation setup in ADS. Adding the 0.2 dB loss to the simulation results as shown in Figure 7.10(b) obtains an excellent agreement with the measured noise figure indicated by the red line. The noise figure is measured to be equal to 0.87 dB at 500 MHz and equal to 0.98 dB at 700 MHz.

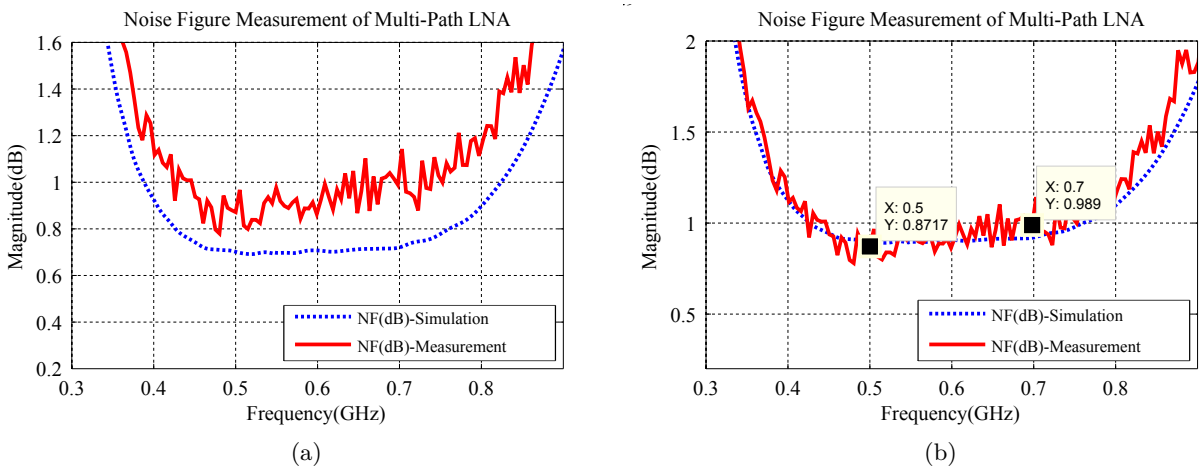


Figure 7.10: Noise Figure of Multi-Path LNA (a) Simulation vs Measurement (b) SMA-Noise included

7.4 Conclusion

This chapter presented two measurement techniques with the Y-factor and cold source method. A more accurate result in the noise figure is obtained using the cold source method over a wide bandwidth. The wide-band LNA with feedback showed terrific wide-band characteristics with a flat gain profile over the entire bandwidth with a minimum noise figure of 1.2 dB. Excellent agreement between simulation and measurement is achieved for the multi-path LNA demonstrating significant bandwidth improvements with a low noise figure of 0.95 dB.

Chapter 8

Conclusion and Recomendations

This thesis aimed to develop two wide-band LNA's for the SKA-mid frequency range, one using classical low noise amplifier techniques and the other a different multi-path cascading concept for possible bandwidth and noise figure improvements. Chapter 2 showed the noise sources involved for each configuration, where the two-port noise theory was applied to the first wide-band design and the multi-path LNA was analysed using multi-port noise theory with the assistance of the noise correlation matrix.

In chapter 3 the necessary skills were developed to stabilize the transistor over a wide frequency range as well as the incorporation of negative feedback into the design for improved flat gain performance across the operation bandwidth. The LNA's were required to operate over a bandwidth of 3:1, two sophisticated matching techniques were presented in chapter 4,one for real impedances and the other for complex impedances to be able to adapt to the optimum noise impedance of the low noise amplifier.

The techniques developed in chapters 2, 3 and 4 were combined and lead to the analysis and design of several wide band low noise amplifiers using different bandwidths in chapter 5, demonstrating the trade off between bandwidth, flat gain response and low noise figure over a bandwidth of 3:1. Good over all performance with no feedback was achieved from 300-600 MHz. As the bandwidth is increased to 900 MHz to meet the SKA requirements the gain started attenuating and caused a big ripple in the passband because the matching networks reached there limit and the only way to maintain the flat gain response was to increase the order of the matching network and sacrifice the performance in the noise figure. The alternative approach was to include feedback in the design in order to maintain the flat gain response, this increased the complexity of the design, since the feedback network introduced several stability issues, but overall a improved flat gain response of 19 dB was achieved and a minimum noise figure of 1.2 dB.

Chapter 6 introduced the multi-path amplifier concept where two amplifiers with no feedback were connected in parallel, each operating at a different frequency. The challenge in the multi-path configuration was to design the input and output matching networks, where sophisticated optimization schemes were needed in order to overcome the complex coupling between the two signal paths. The prototype showed promise in flat gain response from 500-700 MHz and bandwidth improvements compared to a single frequency amplifier design and 0.2 dB lower noise figure than the 300-600 MHz design. Further investigation in the design of multi-path amplifiers

is needed because the process of developing such a structure becomes more complex when more signal paths are added to the configuration.

Two measurement techniques were performed in chapter 7 explaining the advantages of the cold source method compared to the classic Y-factor method. The PNA-X with the cold noise measurement setup showed excellent comparison between the simulation and measurements for both amplifiers. It is therefore critical in future designs to use a spice-model instead of a S-parameter block with limited noise data in order to accurately predict the noise performance of the wide-band LNA's.

Appendix A

BFP842ESD Transistor Data

A.1 Data Sheet Extracts

AC Characteristics, V_{CE} = 2.5 V, f = 0.45 GHz						
Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**
		Min.	**Typ.**	**Max.**		
Power Gain					dB	
Maximum power gain	G_{ms}	–	33	–		I_C = 15 mA
Transducer gain	$\|S_{21}\|^2$	–	29.5	–		I_C = 15 mA
Minimum Noise Figure					dB	
Minimum noise figure	NF_{min}	–	0.4	–		I_C = 5 mA
Associated gain	G_{ass}	–	26	–		I_C = 5 mA
Linearity					dBm	$Z_S = Z_L$ = 50 Ω
1 dB compression point at output	OP_{1dB}	–	6.5	–		I_C = 15 mA
3rd order intercept point at output	$OIP3$	–	22	–		I_C = 15 mA

Table A.1: AC Characteristics of BFP842 HBT [40]

DC Characteristics at T_A = 25 °C						
Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**
		Min.	**Typ.**	**Max.**		
Collector emitter breakdown voltage	$V_{(BR)CEO}$	3.25	3.7		V	I_C = 1 mA, I_B = 0 Open base
Collector emitter leakage current	I_{CES}			400	nA	V_{CE} = 2 V, V_{BE} = 0 E-B short circuited
Collector base leakage current	I_{CBO}			400	nA	V_{CB} = 2 V, I_E = 0 Open emitter
Emitter base leakage current	I_{EBO}			10	µA	V_{EB} = 0.5 V, I_C = 0 Open collector
DC current gain	h_{FE}	150	260	450		V_{CE} = 2.5 V, I_C = 15 mA Pulse measured

Table A.2: DC characteristics of BFP842 HBT [40]

f(GHz)	S11(MAG)	S11(ANG)	S21(MAG)	S21(MAG)	S12(MAG)	S12(ANG)	S22(MAG)	S22(ANG)
0.030	0.9384	-1.4	15.592	177.9	0.0008	164.4	0.9946	-1.0
0.040	0.9375	-1.9	15.550	177.2	0.0004	36.2	0.9952	-1.3
0.050	0.9379	-2.7	15.452	176.4	0.0036	38.7	0.9948	-2.0
0.060	0.9338	-3.1	15.693	175.9	0.0030	102.3	0.9996	-1.8
0.070	0.9386	-3.1	15.538	175.5	0.0007	57.7	0.9952	-2.4
0.080	0.9379	-3.8	15.575	174.8	0.0019	124.8	0.9941	-2.7
0.090	0.9364	-4.5	15.375	174.6	0.0055	92.4	0.9942	-3.2
0.100	0.9343	-4.9	15.512	174.0	0.0056	108.0	0.9941	-3.8
0.110	0.9337	-5.5	15.646	173.1	0.0055	65.1	0.9938	-3.9
0.120	0.9345	-6.1	15.557	172.8	0.0034	106.4	0.9964	-4.5
0.130	0.9353	-6.4	15.437	172.1	0.0052	99.1	0.9916	-4.9
0.140	0.9331	-6.9	15.478	171.7	0.0064	99.8	0.9942	-5.3
0.150	0.9310	-7.5	15.533	171.0	0.0063	87.1	0.9919	-5.7
0.200	0.9258	-9.8	15.415	168.4	0.0079	93.6	0.9899	-7.6
0.250	0.9198	-12.3	15.393	165.4	0.0099	76.8	0.9836	-9.5
0.300	0.9132	-14.8	15.204	162.5	0.0121	79.1	0.9809	-11.3
0.350	0.9061	-17.2	15.112	159.7	0.0142	75.1	0.9740	-13.2
0.400	0.8957	-19.4	14.939	156.9	0.0162	78.5	0.9650	-14.9
0.450	0.8842	-21.9	14.763	154.1	0.0178	73.1	0.9560	-16.7
0.500	0.8742	-24.0	14.627	151.5	0.0201	72.6	0.9482	-18.4
0.600	0.8484	-28.3	14.174	146.3	0.0234	69.6	0.9286	-21.8
0.700	0.8216	-32.4	13.771	141.4	0.0261	67.9	0.9078	-24.9
0.800	0.7916	-36.4	13.324	136.4	0.0300	64.5	0.8856	-28.0
0.900	0.7628	-40.2	12.873	131.9	0.0323	61.6	0.8632	-30.9
1.000	0.7328	-43.8	12.426	127.5	0.0352	59.7	0.8417	-33.6
1.100	0.7036	-47.2	11.971	123.3	0.0378	57.4	0.8198	-36.1
1.200	0.6744	-50.6	11.513	119.3	0.0399	56.3	0.7994	-38.6
1.300	0.6470	-53.6	11.092	115.6	0.0425	53.9	0.7784	-41.0

Table A.3: S-parameters extract of BFP842 HBT [40]

f(GHz)	NFmin(dB)	Gamma_opt(MAG)	Gamma_opt(ANG)	Rn/50
0.450	0.41	0.38	3	0.11
0.900	0.43	0.40	8	0.11
1.500	0.46	0.41	19	0.11
1.900	0.48	0.39	29	0.11
2.400	0.52	0.36	42	0.10
3.500	0.63	0.26	79	0.08
4.000	0.66	0.22	100	0.08
5.000	0.72	0.20	119	0.07
5.500	0.84	0.18	145	0.07
6.000	0.97	0.16	155	0.08

Table A.4: Noise data extract of BFP842 HBT [40]

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